BR1513/D
Rev. 1, Jan-2000

ECLinPS Plus™ Device Data

ON Semiconductor
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ECLinPS Plus™ Device Data

Advanced ECL in Picoseconds

BR1513/D
Rev. 1, Jan–2000

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JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5740–2745
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

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Table of Contents

Data Sheets

MC10EP01

4-Input OR/NOR

The MC10EP01 is a 4–input OR/NOR gate. The device is functionally equivalent to the EL01 device, LVEL01, and E101 (a quad version). With AC performance much faster than the LVEL01 device, the EP01 is ideal for applications requiring the fastest AC performance available.

- 230ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 115 devices

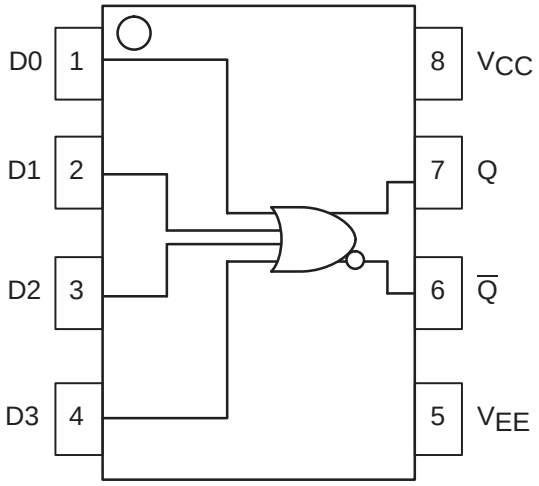

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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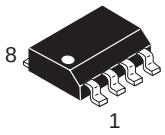

SO–8
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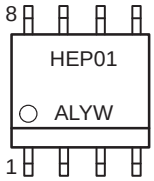
CASE 751

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0–D3	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE

D0	D1	D2	D3	Q	$\overline{Q}$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC10EP01D	SOIC	98 Units/Rail
MC10EP01DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	24	31	20	24	31	20	24	31	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	–150			–150			–150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC} –2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	20	24	31	20	24	31	20	24	31	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	–150			–150			–150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC} –2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	20	24	31	20	24	31	20	24	31	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	–150			–150			–150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC} –2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V) or (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay D –>Q, $\overline{Q}$	100	225	300	150	200	250	200	250	300	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 11.)		TBD TBD			TBD TBD			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise and Fall Times (20% – 80%) Q, $\overline{Q}$	70	120	170	80	130	180	100	150	200	ps

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions.

MC10EP05

2-Input Differential AND/NAND

The MC10EP05 is a 2–input differential AND/NAND gate. The device is functionally equivalent to the EL05 and LVEL05 devices. With AC performance much faster than the LVEL05 device, the EP05 is ideal for applications requiring the fastest AC performance available.

- 170ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 137 devices

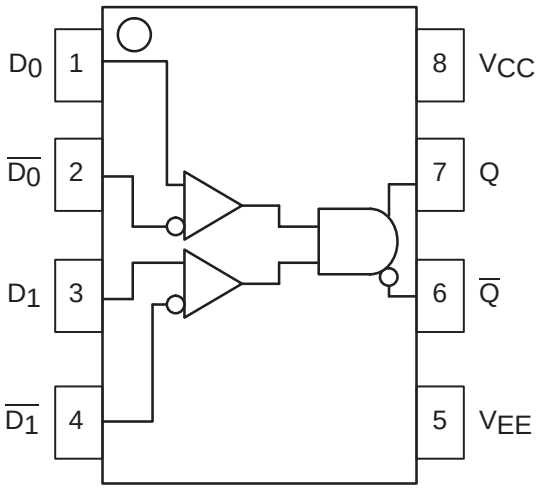


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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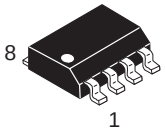

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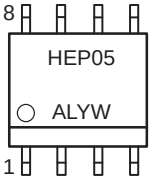
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0, D1, $\overline{D0}$, $\overline{D1}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE

D0	D1	$\overline{D0}$	$\overline{D1}$	Q	$\overline{Q}$
L	L	H	H	L	H
L	H	H	L	L	H
H	L	L	H	L	H
H	H	L	L	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC10EP05D	SOIC	98 Units/Rail
MC10EP05DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	24	29	20	24	29	20	24	29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	20	24	29	20	24	29	20	24	29	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	20	24	29	20	24	29	20	24	29	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	100	160	220	110	170	230	160	220	280	ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	70	120	170	80	130	180	100	150	200	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP08

Differential 2-Input XOR/XNOR

The MC10EP08 is a differential XOR/XNOR gate. The EP08 is ideal for applications requiring the fastest AC performance available.

- 200ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count: 135 devices

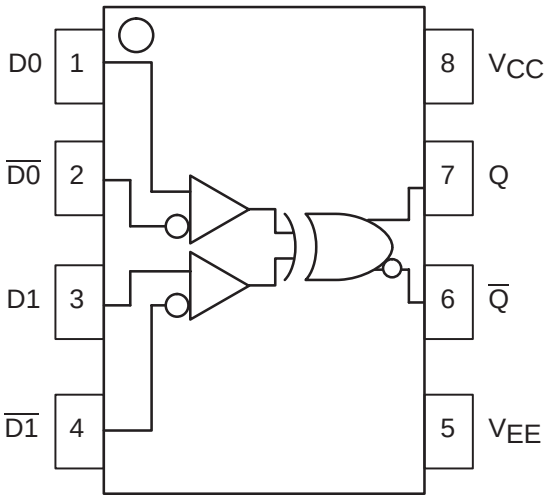


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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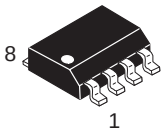
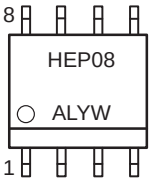


SO–8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0, D1, $\overline{D0}$, $\overline{D1}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE

D0	D1	$\overline{D0}$	$\overline{D1}$	Q	$\overline{Q}$
L	L	H	H	L	H
L	H	H	L	H	L
H	L	L	H	H	L
H	H	L	L	L	H

ORDERING INFORMATION

Device	Package	Shipping
MC10EP08D	SOIC	98 Units/Rail
MC10EP08DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	28	36	20	30	38	20	32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	20	28	36	20	30	38	20	32	38	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	20	28	36	20	30	38	20	32	38	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay (Diff.) D, $\overline{D}$–>Q, $\overline{Q}$	100	170	240	120	200	260	150	220	300	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 14.)		TBD TBD			TBD TBD			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise and Fall Times (20% – 80%) Q, $\overline{Q}$	70	120	170	80	130	180	100	150	200	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions.

MC10EP11

1:2 Differential Fanout Buffer

The MC10EP11 is a differential 1:2 fanout buffer. The device is pin and functionally equivalent to the LVEL11 device. With AC performance much faster than the LVEL11 device, the EP11 is ideal for applications requiring the fastest AC performance available.

- 220ps Typical Propagation Delay
- High Bandwidth to 3 GHz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Outputs will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 73 devices

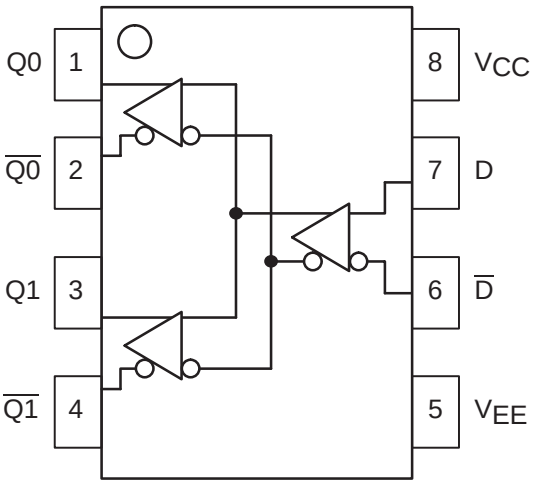


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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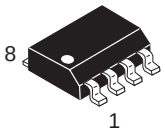

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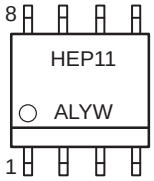
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D, $\overline{D}$	ECL Data Inputs
Q0, $\overline{Q0}$, Q1, $\overline{Q1}$	ECL Data Outputs

ORDERING INFORMATION

Device	Package	Shipping
MC10EP11D	SOIC	98 Units/Rail
MC10EP11DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay (Diff.) CLK–>Q, $\overline{Q}$	140	200	270	160	220	300	180	240	320	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 14.)		TBD TBD			TBD TBD			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$	50	110	180	60	120	200	70	140	220	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions.

MC10EP16

Differential Receiver

The MC10EP16 is a differential receiver. The device is functionally equivalent to the EL16 and LVEL16 devices with higher performance capabilities. With output transition times significantly faster than the EL16 and LVEL16, the EP16 is ideally suited for interfacing with high frequency sources.

The EP16 provides a V_{BB} output for either single-ended use or as a DC bias for AC coupling to the device within the package. The V_{BB} pin should be used only as a bias for the EP16 as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to ground via a 0.01µf capacitor.

- 160ps Propagation Delay
- High Bandwidth to 3 GHz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: 4KV HBM, 200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count: 167 devices

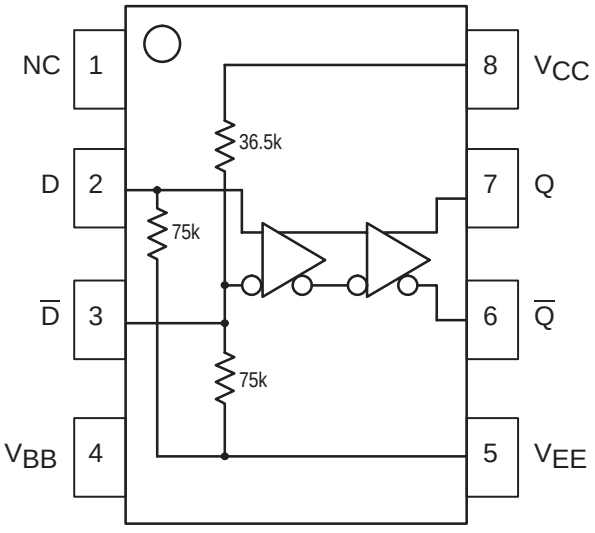


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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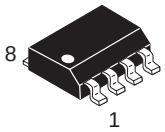

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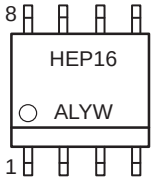
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D, $\overline{D}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{BB}	Ref. Voltage Output

ORDERING INFORMATION

Device	Package	Shipping
MC10EP16D	SOIC	98 Units/Rail
MC10EP16DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	24	31	20	24	31	20	24	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	20	24	31	20	24	31	20	24	32	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	20	24	31	20	24	31	20	24	32	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	100	160	240	100	160	240	120	190	280	ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q	70	120	170	80	130	180	100	150	200	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP31

D Flip Flop with Set and Reset

The MC10EP31 is a D flip flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip–flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

- 275ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 75 devices

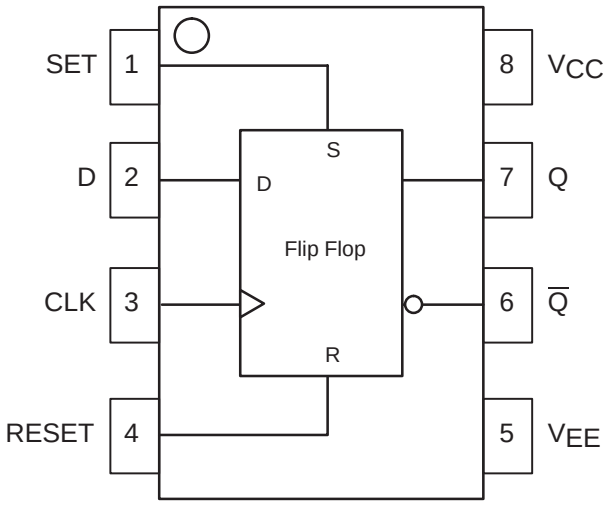


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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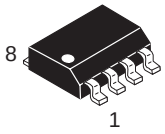

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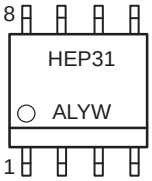
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK	ECL Clock Inputs
Reset	ECL Asynchronous Reset
Set	ECL Asynchronous Set
D	ECL Data Input
Q, $\overline{Q}$	ECL Data Outputs
VCC	Positive Supply
VEE	Negative, 0 Supply

TRUTH TABLE				
D	**SET**	**RESET**	**CLK**	**Q**
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	UNDEF

Z = LOW to HIGH Transition

ORDERING INFORMATION

Device	Package	Shipping
MC10EP31D	SOIC	98 Units/Rail
MC10EP31DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	CLK–>Q, $\overline{Q}$	175	250	325	200	275	350	250	320	400	
	S, R–>Q, $\overline{Q}$	200	280	360	250	330	420	325	400	475	
t_{RR}	Set/Reset Recovery	225	150		200	140		185	130		ps
t_S	Setup Time	150	50		150	50		150	50		ps
t_H	Hold Time	150	50		150	50		150	50		
t_{SKEW}	Duty Cycle Skew (Note 11.)		TBD			TBD			TBD		ps
	Skew Part–to–Part		TBD			TBD			TBD		
t_{PW}	Minimum Pulse Width										ps
	CLK, SET, RESET	550	450		550	450		550	450		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Output Rise/Fall Times										ps
t_f	(20% – 80%) Q, $\overline{Q}$	50	120	180	60	130	200	70	150	220	

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP32

÷2 Divider

The MC10EP32 is an integrated ÷2 divider. The differential clock inputs and the V_{BB} allow a differential, single–ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor.

The reset pin is asynchronous and is asserted on the rising edge. Upon power–up, the internal flip–flops will attain a random state; the reset allows for the synchronization of multiple EP32's in a system.

- 250ps Typical Propagation Delay
- 3 GHz Typical Toggle Frequency
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 78 devices

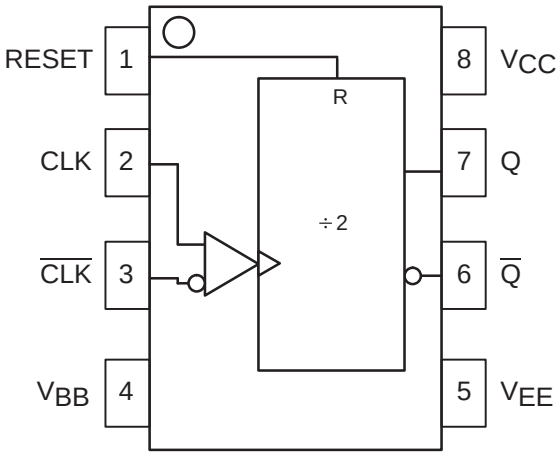


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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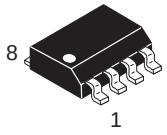

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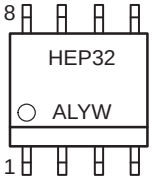
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK, $\overline{CLK}$	ECL Clock Inputs
Reset	ECL Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE				
CLK	**$\overline{CLK}$**	**RESET**	**Q**	**$\overline{Q}$**
X	X	Z	L	H
Z	$\overline{Z}$	L	F	F

Z = LOW to HIGH Transition
$\overline{Z}$ = HIGH to LOW Transition
F = Divide by 2 Function

ORDERING INFORMATION

Device	Package	Shipping
MC10EP32D	SOIC	98 Units/Rail
MC10EP32DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

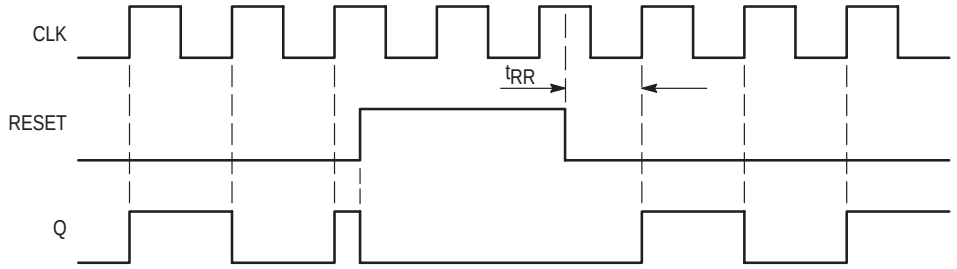


Figure 2. Timing Diagram

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	23	30	37	23	30	37	23	30	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	23	30	37	23	30	37	23	30	37	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	23	30	37	23	30	37	23	30	37	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 13.)	2.5	3.0		2.5	3.0		2.5	3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK–>Q, $\overline{Q}$ RESET–>Q, $\overline{Q}$	100 100	220 220	300 300	100 100	250 250	350 350	180 180	290 290	400 400	ps
t_{RR}	Set/Reset Recovery	200	175		200	175		200	175		ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{PW}	Minimum Pulse Width RESET	550	475		550	475		550	475		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	50	100	150	70	120	170	70	130	200	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP33

÷4 Divider

The MC10EP33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single–ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor.

The reset pin is asynchronous and is asserted on the rising edge. Upon power–up, the internal flip–flops will attain a random state; the reset allows for the synchronization of multiple EP33's in a system.

- 320ps Propagation Delay
- 3 GHz Typical Toggle Frequency
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 91 devices

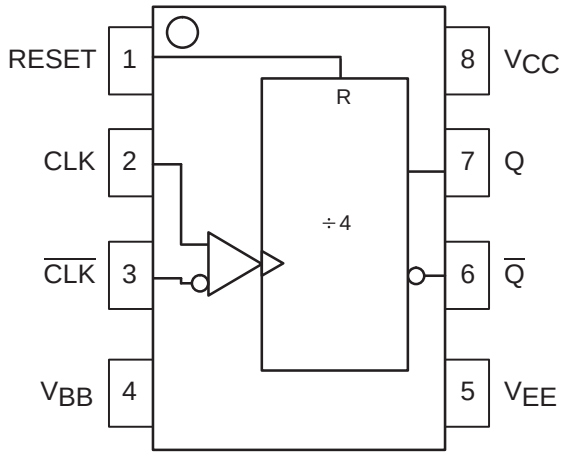


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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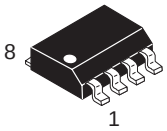

SO–8
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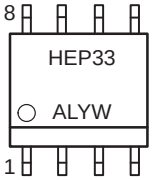
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK, $\overline{CLK}$	ECL Clock Inputs
Reset	ECL Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE				
CLK	**$\overline{CLK}$**	**RESET**	**Q**	**$\overline{Q}$**
X Z	X $\overline{Z}$	Z L	L F	H F

Z = LOW to HIGH Transition
$\overline{Z}$ = HIGH to LOW Transition
F = Divide by 4 Function

ORDERING INFORMATION

Device	Package	Shipping
MC10EP33D	SOIC	98 Units/Rail
MC10EP33DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

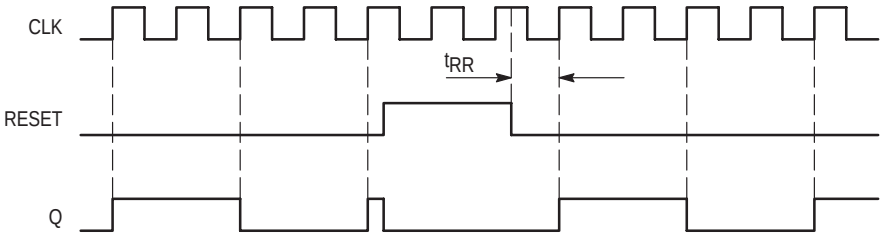


Figure 2. Timing Diagram

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	18	26	34	18	26	34	18	26	34	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	18	26	34	18	26	34	18	26	34	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	18	26	34	18	26	34	18	26	34	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 13.)	2.5	3.0		2.5	3.0		2.5	3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to CLK/Q Output Differential RESET/Q	225 200	300 270	360 360	250 250	320 320	380 380	275 275	350 350	425 425	ps
t_{RR}	Set/Reset Recovery	300	225		300	225		300	225		ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0	20		5.0	20		5.0	20	ps
t_{PW}	Minimum Pulse Width RESET	550	480		550	480		550	480		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	90	170	200	100	180	250	120	200	280	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP35

JK Flip Flop

The MC10EP35 is a higher speed/low voltage version of the EL35 JK flip flop. The J/K data enters the master portion of the flip flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

- 300ps Propagation Delay
- High Bandwidth to 3 GHz Typical
- High Bandwidth Output Transistors
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 77 devices

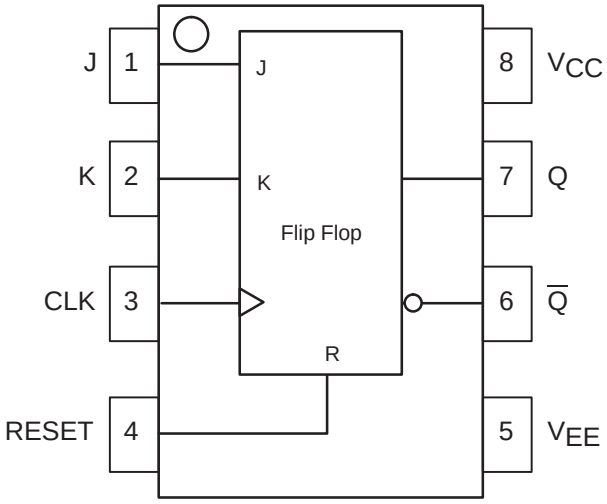


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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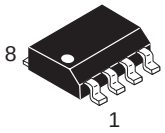

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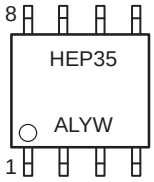
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK	ECL Clock Inputs
J, K	ECL Signal Inputs
RESET	ECL Asynchronous Reset
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE				
J	K	RESET	CLK	Qn+1
L	L	L	Z	Qn
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\overline{Qn}$
X	X	H	X	L

Z = LOW to HIGH Transition

ORDERING INFORMATION

Device	Package	Shipping
MC10EP35D	SOIC	98 Units/Rail
MC10EP35DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	30	40	50	30	40	50	30	40	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	30	40	50	30	40	50	30	40	50	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	30	40	50	30	40	50	30	40	50	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Diff. R, CLK–>Q, $\overline{Q}$	150	300	450	170	320	470	180	330	480	ps
t_{RR}	Set/Reset Recovery		TBD			TBD			TBD		ps
t_S t_H	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps
t_{SKEW}	Duty Cycle Skew (Note 11.) Skew Part–to–Part		TBD TBD			TBD TBD			TBD TBD		ps
t_{PW}	Minimum Pulse Width CLK, RESET		400			400			400		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$	50	110	180	60	120	200	70	140	220	ps

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP56

Product Preview

Dual Differential 2:1 Multiplexer

The MC10EP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling of input signals. If used, the V_{BB} output should be bypassed to ground with a 0.01µF capacitor.

The device features both individual and common select inputs to address both data path and random logic applications.

- 350ps Typical Propagation Delays
- Typical Frequency 3.0GHz
- 20–Lead TSSOP Package
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Separate and Common Select
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Outputs
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 140 devices

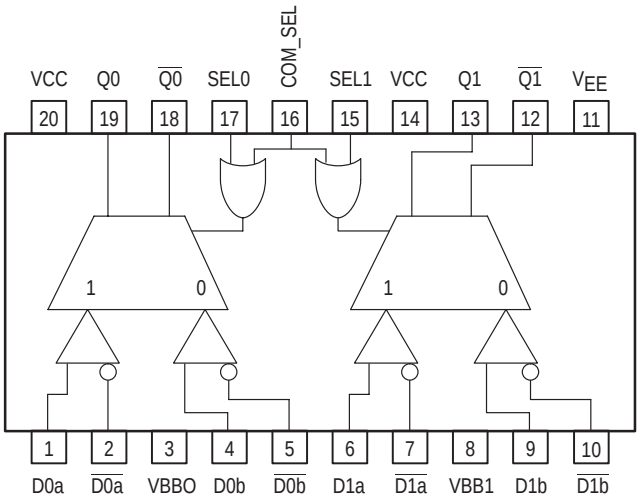


Figure 1. 20–Lead TSSOP (Top View) **and Logic Diagram**

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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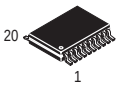
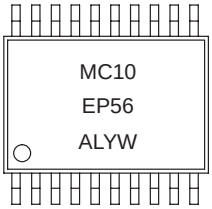


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0a–D1a	ECL Input Data a
$\overline{D0a}$–$\overline{D1a}$	ECL Input Data a Invert
D0b–D1b	ECL Input Data b
$\overline{D0b}$–$\overline{D1b}$	ECL Input Data b Invert
SEL0–SEL1	ECL Indiv. Select Input
COM_SEL	ECL Common Select Input
V_{BB0}, V_{BB1}	Output Reference Voltage
Q0–Q1	ECL True Outputs
$\overline{Q0}$–$\overline{Q1}$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

ORDERING INFORMATION

Device	Package	Shipping
MC10EP56DT	TSSOP	75 Units/Rail
MC10EP56DTR2	TSSOP	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	140 100	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)		°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 5.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 9.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	D–>Q, $\overline{Q}$ (Diff)		TBD			340			TBD		
	D–>Q, $\overline{Q}$ (SE)		TBD			340			TBD		
	SEL–>Q, $\overline{Q}$		TBD			410			TBD		
	COM_SEL–>Q, $\overline{Q}$		TBD			410			TBD		
t_{SKEW}	Within–Device Skew (Note 14.)		TBD			TBD			TBD		ps
	Duty Cycle Skew (Note 15.)		TBD			TBD			TBD		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r	Output Rise/Fall Times Q, $\overline{Q}$		TBD			120			TBD		ps
t_f	(20% – 80%) Q, $\overline{Q}$		TBD			110			TBD		

13. F_{max} guaranteed for functionality only. See Figure 2 for typical output swing. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Within–Device Skew is defined as identical transitions on similar paths through a device.
15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP57, MC100EP57

Product Preview

4:1 Differential Multiplexer

The MC10/100EP57 is a fully differential 4:1 multiplexer. By leaving the SEL1 line open (pulled LOW via the input pulldown resistors) the device can also be used as a differential 2:1 multiplexer with SEL0 input selecting between D0 and D1. The fully differential architecture of the EP57 makes it ideal for use in low skew applications such as clock distribution.

The SEL1 is the most significant select line. The binary number applied to the select inputs will select the same numbered data input (i.e., 00 selects D0).

Multiple V_{BB} outputs are provided for single-ended or AC coupled interfaces. In these scenarios, the V_{BB} output should be connected to the data bar inputs and bypassed via a 0.01μF capacitor to ground. Note that the V_{BB} output can source/sink up to 0.5mA of current without upsetting the voltage level. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation

- 350ps Typical Propagation Delays
- Typical Frequency 3.0GHz
- 20–Lead TSSOP Package
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >2KV HBM, >100V MM
- V_{BB} Outputs
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Useful as Either 4:1 or 2:1 Multiplexer
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 584 devices

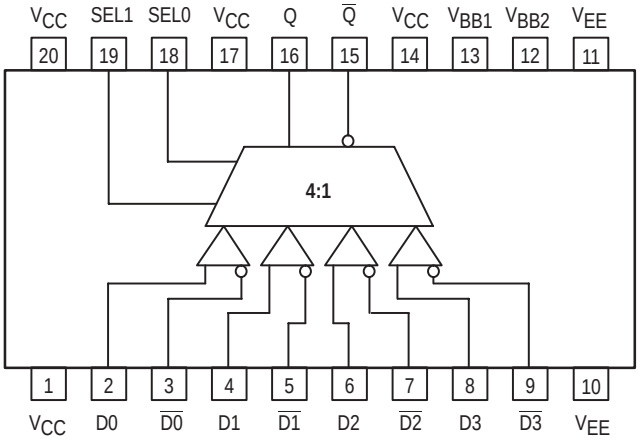


Figure 1. 20–Lead TSSOP (Top View) **and Logic Diagram**

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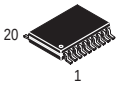
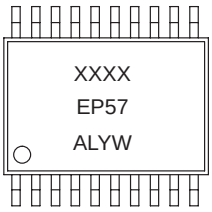


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



XXXX = MC10 or 100

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0–3, $\overline{D0–3}$	ECL Diff. Data Inputs
SEL0, 1	ECL Mux Select Inputs
V_{BB1}, V_{BB2}	ECL Reference Output Voltage
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

FUNCTION TABLE

SEL1	SEL0	DATA OUT
L	L	D0, $\overline{D0}$
L	H	D1, $\overline{D1}$
H	L	D2, $\overline{D2}$
H	H	D3, $\overline{D3}$

ORDERING INFORMATION

Device	Package	Shipping
MC10EP57DT	TSSOP	75 Units/Rail
MC10EP57DTR2	TSSOP	2500 Tape & Reel
MC100EP57DT	TSSOP	75 Units/Rail
MC100EP57DTR2	TSSOP	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	140 100	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	23 to 41 ±5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)					48					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — SEL, D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					48					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)					48					mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	D–>Q, $\overline{Q}$ (Diff)		TBD			350			TBD		
	D–>Q, $\overline{Q}$ (SE)		TBD			350			TBD		
	SEL–>Q, $\overline{Q}$		TBD			410			TBD		
	COM_SEL–>Q, $\overline{Q}$		TBD			410			TBD		
t_{SKEW}	Within–Device Skew (Note 14.)		TBD			TBD			TBD		ps
	Duty Cycle Skew (Note 15.)		TBD			TBD			TBD		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r	Output Rise/Fall Times Q, $\overline{Q}$		TBD			120			TBD		ps
t_f	(20% – 80%) Q, $\overline{Q}$		TBD			110			TBD		

13. F_{max} guaranteed for functionality only.
14. Within–Device Skew is defined as identical transitions on similar paths through a device.
15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP58

2:1 Multiplexer

The MC10EP58 is a 2:1 multiplexer. The device is pin and functionally equivalent to the EL58 and LVEL58 devices.

- 275ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 41 devices

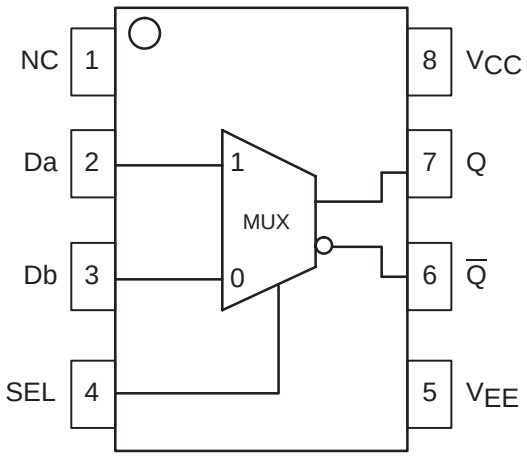


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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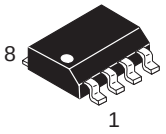
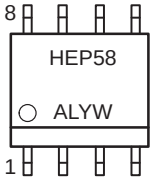


SO–8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Da, Db	ECL Data Inputs
SEL	ECL Select Inputs
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE	
SEL	**Data**
H L	a b

ORDERING INFORMATION

Device	Package	Shipping
MC10EP58D	SOIC	98 Units/Rail
MC10EP58DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	28	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	20	28	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	20	28	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	D–>Q, $\overline{Q}$	170	250	350	190	275	375	210	300	400	
	SEL–>Q, $\overline{Q}$	170	250	350	190	275	375	210	300	400	
t_{SKEW}	Duty Cycle Skew (Note 11.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	60	120	190	60	130	200	70	150	220	ps

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP89

Coaxial Cable Driver

The MC10EP89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in digital video broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver produces swings 70% larger than a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 (5V) and 1.4V (3.3V) swing allow for termination at both ends of the cable, while maintaining a 800mV (5V) and 700mV (3.3V) swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard V_{CC}–2.0V. All of the DC parameters are tested with a 50Ω to V_{CC}–3.0V load. The driver accepts a standard differential ECL input and can run off of the digital video broadcast standard –5.0V supply.

- 310ps Typical Propagation Delay
- 3.0 GHz Typical Toggle Frequency
- 1.6V (5V) and 1.4V (3.3V) Swing
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 152 devices

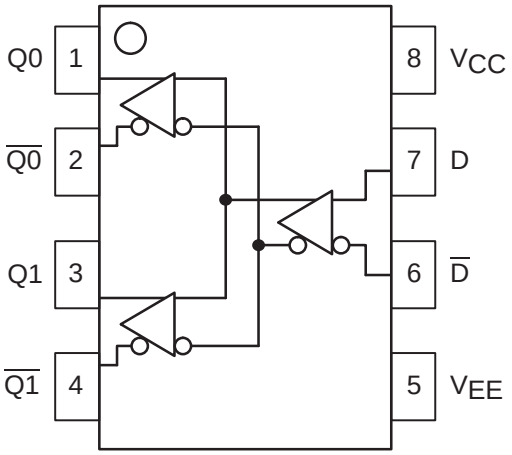


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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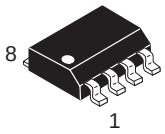
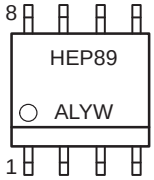


SO–8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D, $\overline{D}$	ECL Data Inputs
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

ORDERING INFORMATION

Device	Package	Shipping
MC10EP89D	SOIC	98 Units/Rail
MC10EP89DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

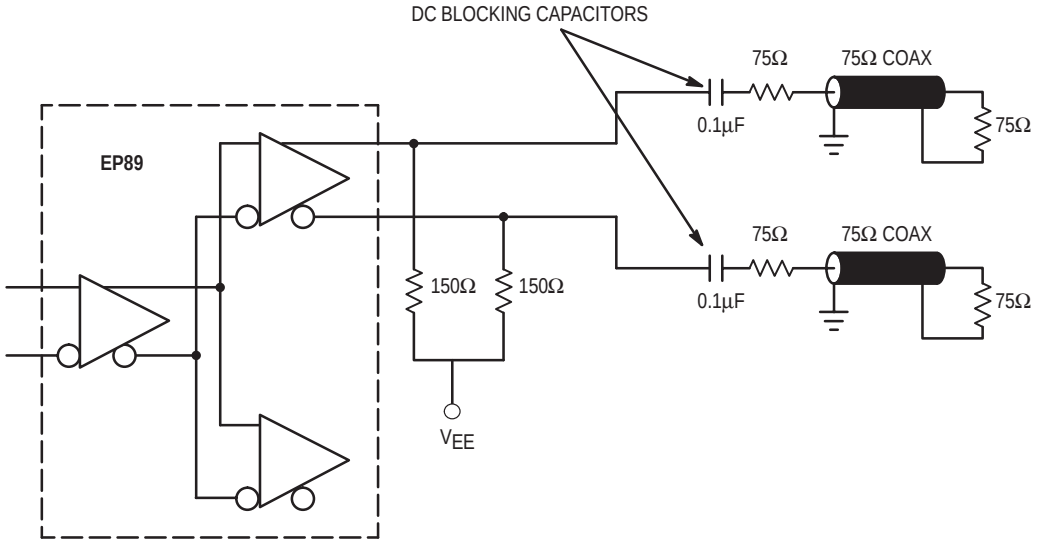


Figure 2. EP89 Termination Configuration

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –3.3 ± 0.01V) (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	22	28	34	24	32	38	28	34	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1220	–1120	–1020	–1150	–1050	–950	–1075	–975	–875	mV
V_{OL}	Output LOW Voltage (Note 2.)	–2680	–2580	–2480	–2670	–2570	–2470	–2630	–2530	–2430	mV
V_{IH}	Input HIGH Voltage Single Ended	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage Single Ended	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	–1.3		0.0	–1.3		0.0	–1.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = –3.3V, all other pins floating.
2. All loading with 50 ohms to V_{CC}–3.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.2 ± 0.01V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	25	32	39	28	35	42	31	38	45	mA
V_{OH}	Output HIGH Voltage (Note 6.)	–1220	–1120	–1020	–1150	–1050	–950	–1075	–975	–875	mV
V_{OL}	Output LOW Voltage (Note 6.)	–2950	–2800	–2650	–2950	–2850	–2650	–2950	–2800	–2650	mV
V_{IH}	Input HIGH Voltage Single Ended	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage Single Ended	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	–3.2		0.0	–3.2		0.0	–3.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 0V, V_{EE} = –5.2V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–3.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.01V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	22	28	34	24	32	38	28	34	40	mA
V_{OH}	Output HIGH Voltage (Note 10.)	2080	2180	2280	2150	2250	2350	2225	2325	2425	mV
V_{OL}	Output LOW Voltage (Note 10.)	620	720	820	630	730	830	670	770	870	mV
V_{IH}	Input HIGH Voltage Single Ended	2070		2410	2170		2490	2240		2580	mV
V_{IL}	Input LOW Voltage Single Ended	1350		1800	1350		1820	1350		1855	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–3.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 16.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 13.)	27	34	41	30	37	44	32	39	46	mA
V_{OH}	Output HIGH Voltage (Note 14.)	3780	3880	3980	3850	3950	4050	3925	4025	4125	mV
V_{OL}	Output LOW Voltage (Note 14.)	2075	2225	2375	2060	2210	2360	2090	2240	2390	mV
V_{IH}	Input HIGH Voltage Single Ended	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage Single Ended	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 15.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

13. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
14. All loading with 50 ohms to V_{CC}–3.0 volts.
15. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
16. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 17.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	200	280	380	220	310	400	250	330	420	ps
t_{SKEW}	Duty Cycle Skew (Note 18.)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.) (Note 19.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120	230	380	130	250	410	150	270	430	ps

17. F_{max} guaranteed for functionality only.
18. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
19. V_{IL} must not go below V_{CC} – 3V.

MC10EP101

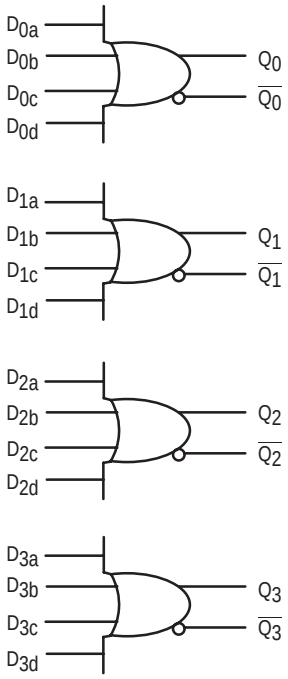
Product Preview

Quad 4-Input OR/NOR

The MC10EP101 is a Quad 4–input OR/NOR gate. The device is functionally equivalent to the E101. With AC performance much faster than the E101 device, the EP101 is ideal for applications requiring the fastest AC performance available. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

- 240ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- ESD Protection: >2KV HBM, >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 173 devices

LOGIC DIAGRAM



This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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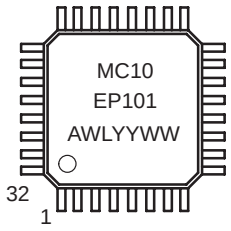
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0a–D3d	ECL Data Inputs
Q0–Q3, $\overline{Q0}$–$\overline{Q3}$	ECL Data Outputs
VCC	Positive Supply
VBB	Reference Voltage Output
VEE	Negative, 0 Supply

TRUTH TABLE

Dna	Dnb	Dnc	Dnd	Qn	$\overline{Qn}$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC10EP101FA	TQFP	250 Units/Tray
MC10EP101FAR2	TQFP	2000 Tape & Reel

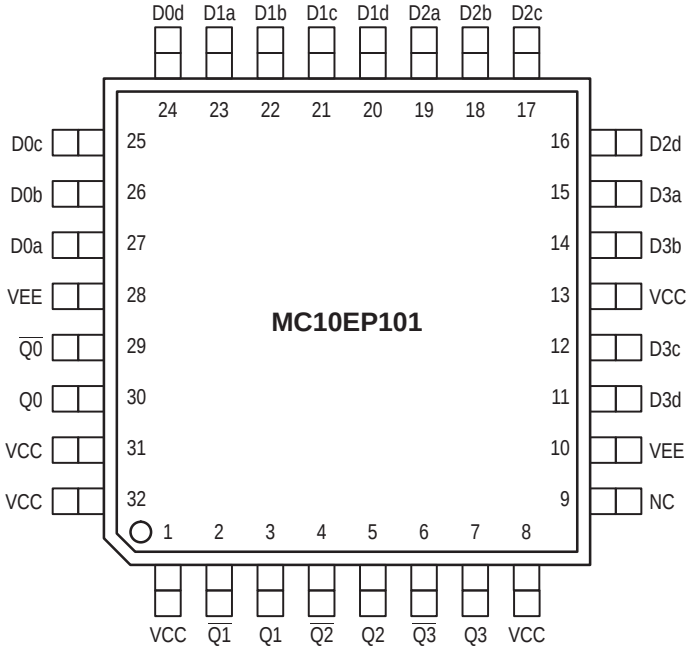


Figure 1. 32–Lead TQFP Pinout
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –5.5V to –3.0V) (Note 3.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					60					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	–150			–150			–150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC} –2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)					60					mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	–150			–150			–150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC} –2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)					60					mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	–150			–150			–150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC} –2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V) or (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay D –>Q, $\overline{Q}$		225			240			250		ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 11.)		TBD TBD			TBD TBD			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise and Fall Times (20% – 80%) Q, $\overline{Q}$					200 135			150		ps

10. F_{max} guaranteed for functionality only.
11. Skew is measured between outputs under identical transitions.

MC10EP105

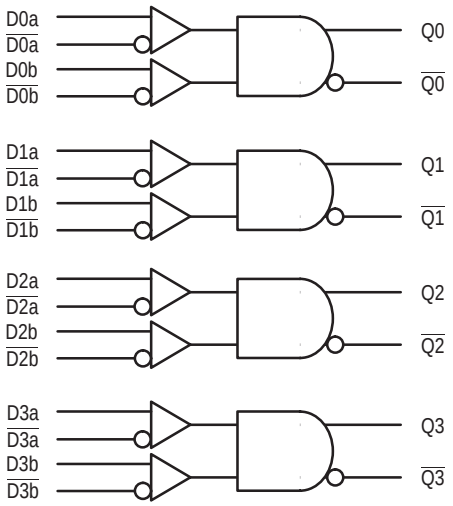
Product Preview

Quad 2-Input Differential AND/NAND

The MC10EP105 is a 2–input differential AND/NAND gate. Each gate is functionally equivalent to a EP05 and LVEL05 devices. With AC performance much faster than the LVEL05 device, the EP105 is ideal for applications requiring the fastest AC performance available. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

- 190ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- Internal Input Pulldown Resistors
- ESD Protection: >2KV HBM, >100V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 444 devices

LOGIC DIAGRAM



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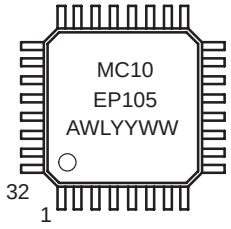
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Dna, Dnb, $\overline{\text{Dna}}$, $\overline{\text{Dnb}}$	ECL Data Inputs
Qn, $\overline{\text{Qn}}$	ECL Data Outputs
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

TRUTH TABLE

Dna	Dnb	$\overline{\text{Dna}}$	$\overline{\text{Dnb}}$	Qn	$\overline{\text{Qn}}$
L	L	H	H	L	H
L	H	H	L	L	H
H	L	L	H	L	H
H	H	L	L	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC10EP105FA	TQFP	250 Units/Tray
MC10EP105FAR2	TQFP	2000 Tape & Reel

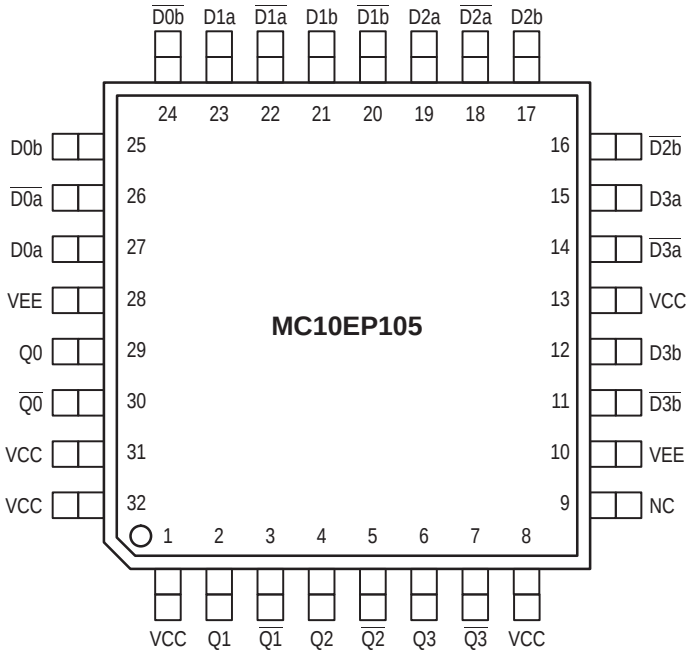


Figure 1. 32–Lead TQFP Pinout
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					59					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					59					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)					59					mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential					190					ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)					120					ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP116, MC100EP116

Product Preview

Hex Differential Line Receiver

The MC10EP116/100EP116 is a 6-bit differential line receiver based on the EP16 device. The 3.0GHz bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

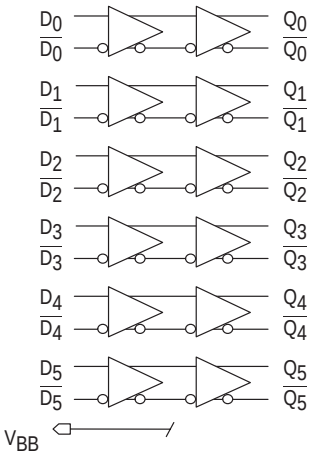
A V_{BB} pin is available to AC couple an input signal to the device. More information on AC coupling can be found in the design handbook interfacing with ECLinPS on our website.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below V_{CC}. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

- 230ps Typical Propagation Delay
- High Bandwidth to 3.0 GHz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: 2KV HBM, 100V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count: 729 devices

LOGIC DIAGRAM



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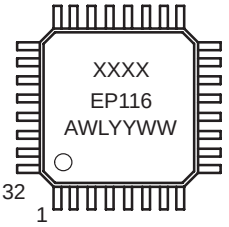
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



XXXX = MC10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D[0:5], $\overline{D[0:5]}$	ECL Differential Data Inputs
Q[0:5], $\overline{Q[0:5]}$	ECL Differential Data Outputs
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

ORDERING INFORMATION

Device	Package	Shipping
MC10EP116FA	TQFP	250 Units/Tray
MC10EP116FAR2	TQFP	2000 Tape & Reel
MC100EP116FA	TQFP	250 Units/Tray
MC100EP116FAR2	TQFP	2000 Tape & Reel

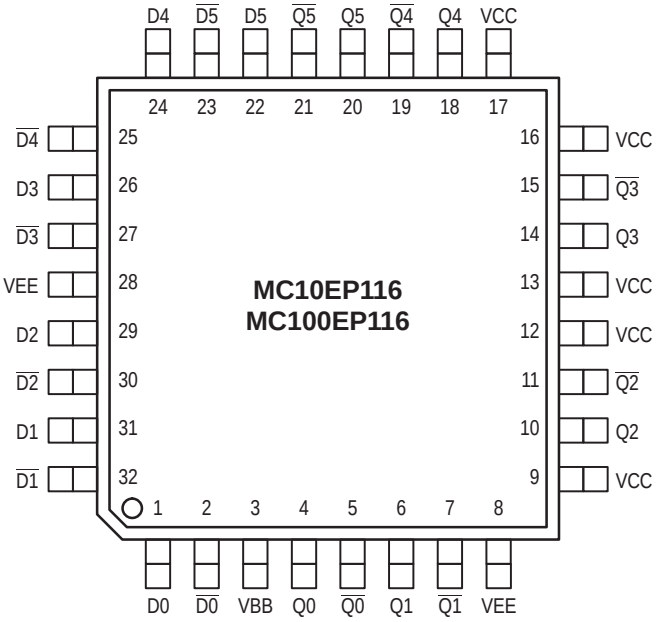


Figure 1. 32–Lead LQFP Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					80					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					80					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)					80					mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential					230					ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)					130					ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC100EP139

Product Preview

÷2/4, ÷4/5/6 Clock Generation Chip

The MC100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single–ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single–ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip–flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip–flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

- 50ps Output–to–Output Skew
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >2KV HBM, >100V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 758 devices

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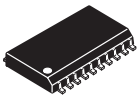
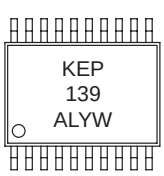
TSSOP–20
DT SUFFIX
CASE 948E



SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP139DT	TSSOP	75 Units/Rail
MC100EP139DTR2	TSSOP	2500 Tape/Reel
MC100EP139DW	SOIC	38 Units/Rail
MC100EP139DWR2	SOIC	2500 Tape/Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

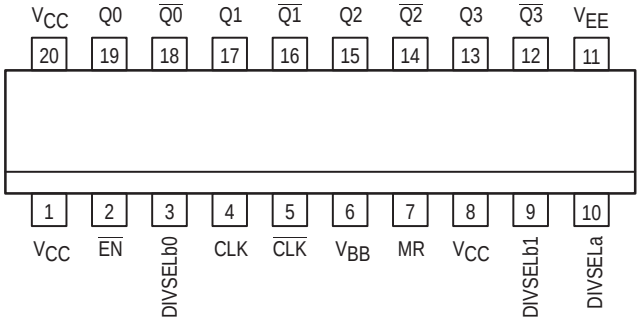


Figure 1. 20–Lead SOIC (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLES

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low–to–High Transition
ZZ = High–to–Low Transition

DIVSELa	Q0:1 OUTPUTS
0	Divide by 2
1	Divide by 4

DIVSELb0	DIVSELb1	Q2:3 OUTPUTS
0	0	Divide by 4
1	0	Divide by 6
0	1	Divide by 5
1	1	Divide by 5

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{Q2}$, $\overline{Q3}$	ECL Diff ÷4/5/6 Outputs
DIVSELa	ECL Freq. Select Input ÷2/4
DIVSELb0	ECL Freq. Select Input ÷4/5/6
DIVSELb1	ECL Freq. Select Input ÷4/5/6
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative, 0 Supply

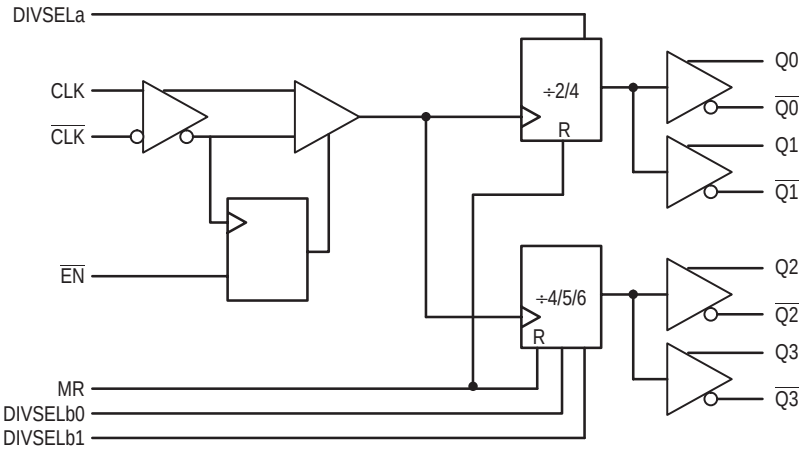


Figure 2. Logic Diagram

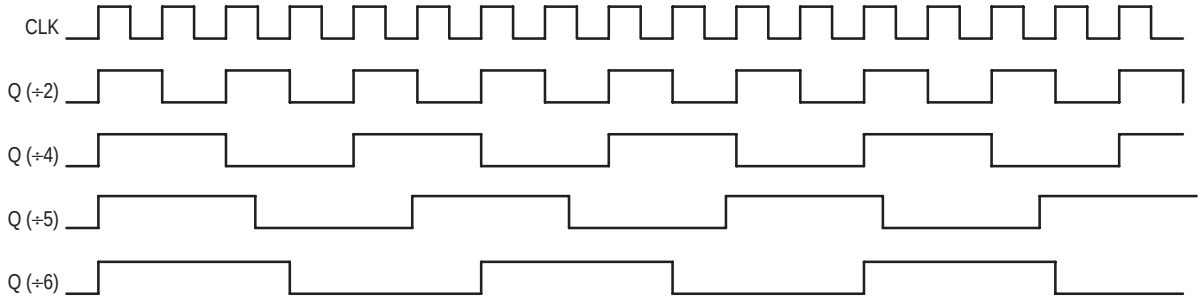


Figure 3. Timing Diagram

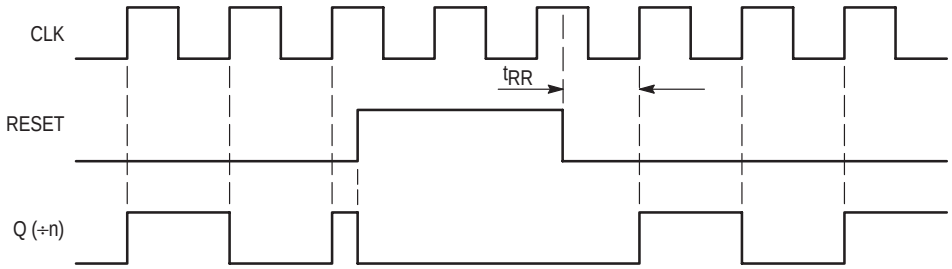


Figure 4. Timing Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA} (DT Suffix)	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	140 100	°C/W
θ_{JC} (DT Suffix)	Thermal Resistance (Junction–to–Case)	23 to 41 ± 5%	°C/W
θ_{JA} (DW Suffix)	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	90 60	°C/W
θ_{JC} (DW Suffix)	Thermal Resistance (Junction–to–Case)	33 to 35 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –5.5V to –3.0V) (Note 3.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1250	–1100	–895	–1250	–1100	–895	–1250	–1100	–895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1995	–1850	–1650	–1995	–1850	–1650	–1995	–1850	–1650	mV
V_{IH}	Input HIGH Voltage Single Ended		–1022			–1022			–1022		mV
V_{IL}	Input LOW Voltage Single Ended		–1642			–1642			–1642		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC} –2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	70	83	100	70	87	105	75	90	110	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2050	2200	2405	2050	2200	2405	2050	2200	2405	mV
V_{OL}	Output LOW Voltage (Note 5.)	1305	1450	1650	1305	1450	1650	1305	1450	1650	mV
V_{IH}	Input HIGH Voltage Single Ended		2277			2277			2277		mV
V_{IL}	Input LOW Voltage Single Ended		1657			1657			1657		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC} –2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3750	3900	4105	3750	3900	4105	3750	3900	4105	mV
V_{OL}	Output LOW Voltage (Note 8.)	3005	3150	3350	3005	3150	3350	3005	3150	3350	mV
V_{IH}	Input HIGH Voltage Single Ended		3977			3977			3977		mV
V_{IL}	Input LOW Voltage Single Ended		3357			3357			3357		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC} –2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V) or (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 10.)	1.0	1.2		1.0	1.2		1.0	1.2		GHz
t_{PLH}, t_{PHL}	Propagation Delay CLK, Q(DIFF) CLK, Q(SE) MR, Q	550	700	800	600	750	900	675	825	975	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 11.)					50 200					ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise and Fall Times Q, $\overline{Q}$ (20% – 80%)	110	180	250	125	190	275	150	215	300	ps
t_s	Setup Time $\overline{EN}$, $\overline{CLK}$ DIVSEL, CLK	200 400	120		200 400	120		200 400	120		ps
t_h	Hold Time $\overline{CLK}$, $\overline{EN}$ CLK, DIVSEL	100 150	50		100 150	50		100 150	50		ps
V_{pp}	Input Voltage Swing (Diff)	300	800	1200	300	800	1200	300	800	1200	mV
t_{rr}	Reset Recovery Time					100					ps
t_{pw}	Minimum Pulse Width CLK MR	550	450		550	450		550	450		ps

10. F_{max} guaranteed for functionality only.
11. Skew is measured between outputs under identical transitions.

MC10EP016

Product Preview

8-Bit Synchronous Binary Up Counter

The MC10EP016 is a high–speed synchronous, presettable, cascadeable 8–bit binary counter. Architecture and operation are the same as the MC10E016 in the ECLinPS™ family.

The counter features internal feedback to $\overline{TC}$ gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all–one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated. COUT and $\overline{COUT}$ have been added so cascading can now be done without adding external components. A differential clock input has also been added to improve signal to noise ratio.

- 1.3GHz Typical Count Frequency
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 550ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- Addition of COUT and $\overline{COUT}$
- 8–Bit
- Differential Clock Input
- VBB Output
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Q Output will default LOW with inputs open or at V_{EE}
- 75kΩ Pulldown Resistors
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 897 devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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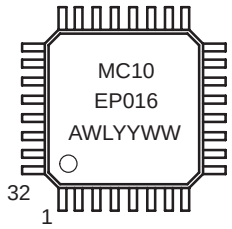
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP016FA	TQFP	250 Units/Tray
MC10EP016FAR2	TQFP	2000 Tape & Reel

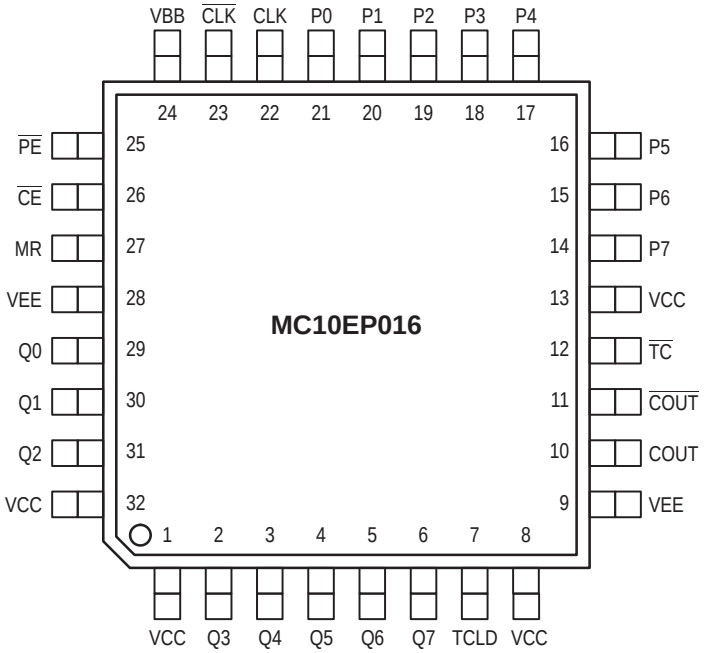


Figure 1. 32–Lead TQFP Pinout
(Top View)

PIN DESCRIPTION	
PIN	**FUNCTION**
P0–P7	ECL Parallel Data (Preset) Inputs
Q0–Q7	ECL Data Outputs
$\overline{CE}$	ECL Count Enable Control Input
$\overline{PE}$	ECL Parallel Load Enable Control Input
MR	ECL Master Reset
CLK, $\overline{CLK}$	ECL Differential Clock
$\overline{TC}$	ECL Terminal Count Output
TCLD	ECL TC–Load Control Input
COUT, $\overline{COUT}$	ECL Carry–Out Output
VCC	Positive Supply
VEE	Negative, 0 Supply
VBB	Reference Voltage Output

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLES

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	FUNCTION
X	L	X	L	Z	Load Parallel (Pn to Qn)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Qn : = LOW, $\overline{TC}$: = HIGH)

ZZ = Clock Pulse (High–to–Low)
Z = Clock Pulse (Low–to–High)

FUNCTION TABLE

Function	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P7–P4	P3	P2	P1	P0	Q7–Q4	Q3	Q2	Q1	Q0	TC	$\overline{COUT}$	COUT
Load Count	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L	L	H
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H	H	L
Load Hold	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
Load on Terminal Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H	H	L
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)					150(4)					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.
4. Recommend 500 lfpm air flow when using –5.2V power supply.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 7.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					150					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 10.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 8.)					150(11)					mA
V_{OH}	Output HIGH Voltage (Note 9.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 9.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

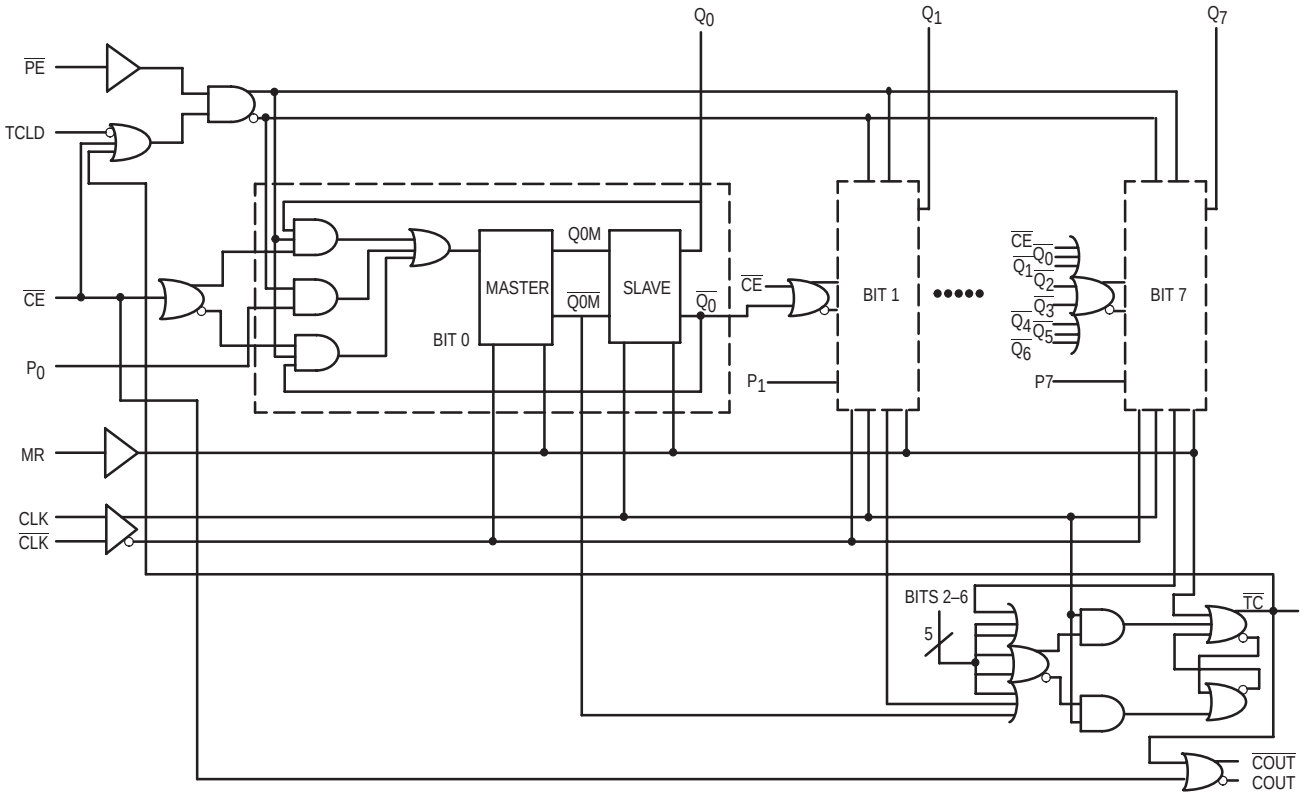
8. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
9. All loading with 50 ohms to V_{CC}–2.0 volts.
10. Input and output parameters vary 1:1 with V_{CC}.
11. Recommend 500 lfpm air flow when using +5V power supply.

AC CHARACTERISTICS (V_{EE} = –3.6V to –3.0; V_{CC} = GND)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Count Frequency (Note 12.)					1.3					GHz
t_{PLH} t_{PHL}	Propagation Delay CLK –> Q MR –> Q CLK –> $\overline{TC}$ MR –> $\overline{TC}$					500 550 550 550					ps
t_S	Setup Time Pn $\overline{CE}$ $\overline{PE}$ TCLD										ps
t_H	Hold Time Pn $\overline{CE}$ $\overline{PE}$ TCLD										ps
t_{RR}	Reset Recovery Time										ps
t_{PW}	Minimum Pulse Width CLK, MR					300					ps
t_r t_f	Output Rise/Fall Times (20% – 80%)					165					ps

12. f_{max} specified to 1.3GHz with reduced output swing.

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

Applications Information

Cascading Multiple EP016 Devices

For applications which call for larger than 8-bit counters multiple EP016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of EP016 devices. Two EP016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorially illustrates the cascading of 4 EP016s to build a 32-bit high frequency counter. Note the EP01 gates used to OR the terminal count outputs of the lower order EP016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant EP016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an EP016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting EP016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary setup time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 1 shows EP01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, LVECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is TBD and that for a 16-bit counter is TBD. Figure 2 shows cascade approach using $\overline{COUT}$ output with no external gates. This may cause a reduced frequency due to internal gate delays.

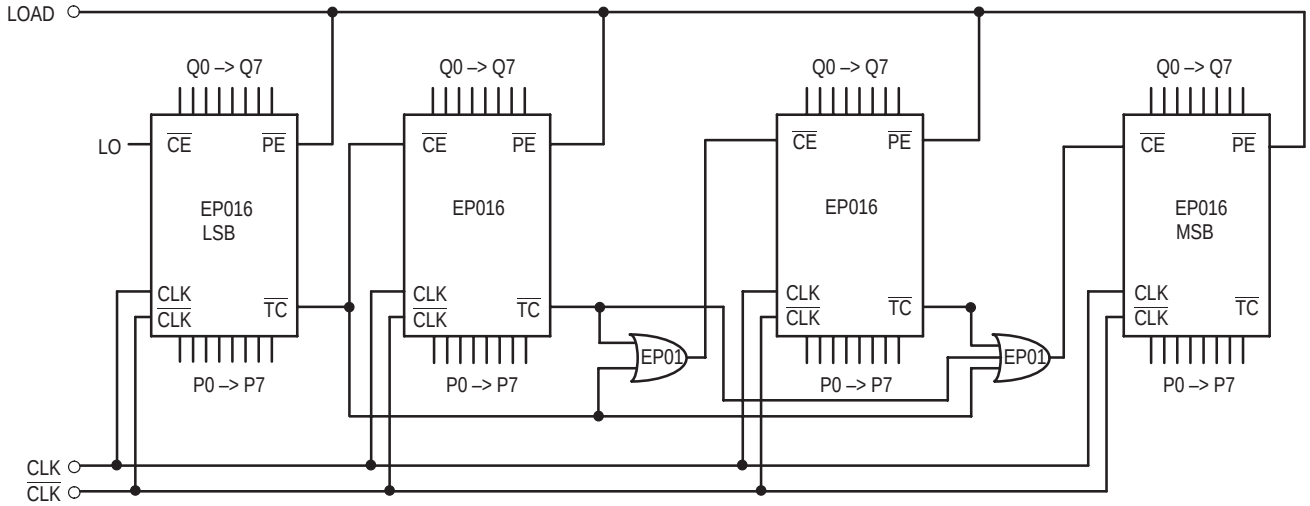


Figure 1. 32-Bit Cascaded EP016 Counter

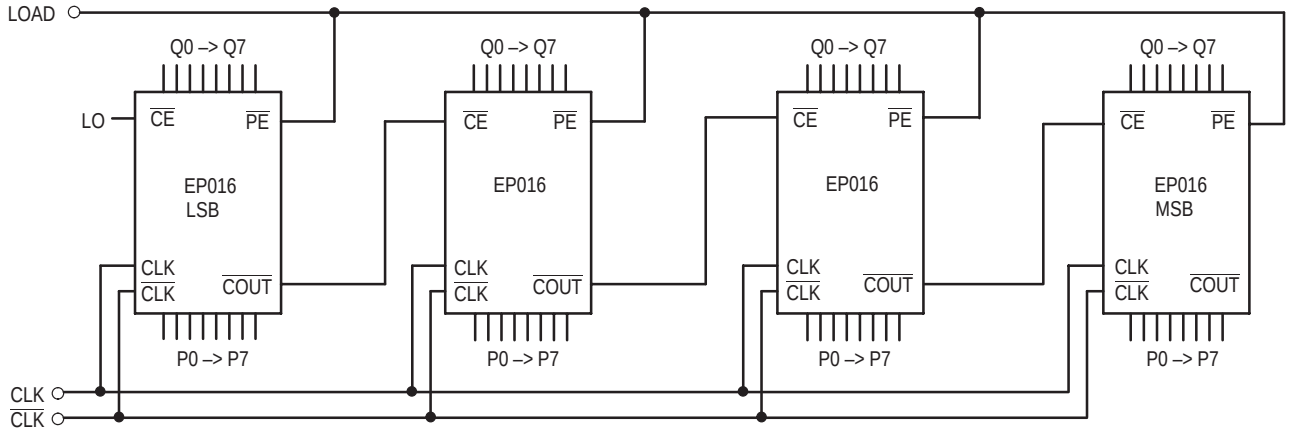


Figure 2. 32-Bit Cascaded EP016 Counter without external gates

Applications Information (continued)

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The EP016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 3 below illustrates the input conditions necessary for utilizing the EP016 as a programmable divider set up to divide by 113.

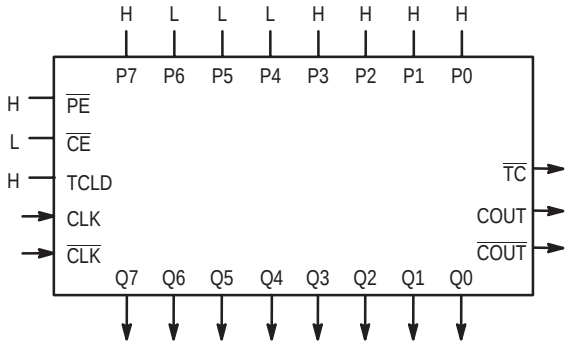


Figure 3. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 – 113 = $8F_{16}$ = 1000 1111

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 3 will result in the waveforms of Figure 4. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 1. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single EP016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016s can be cascaded in a manner similar to that already discussed. When EP016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple EP016 divider chains.

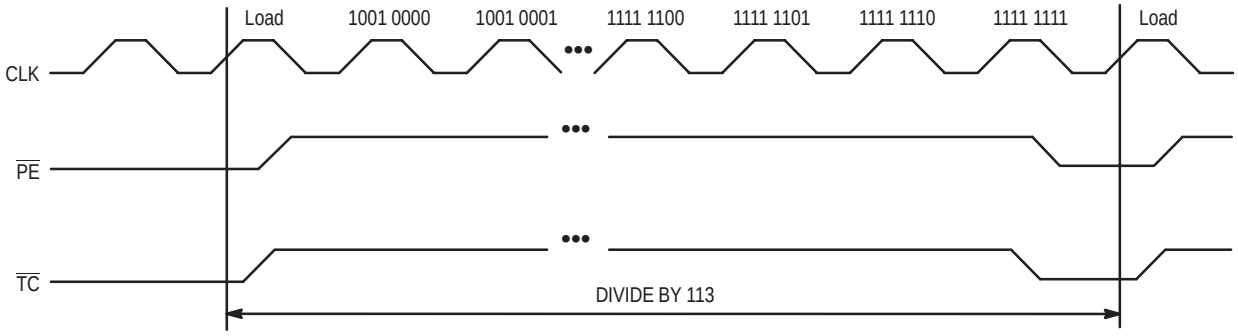


Figure 4. Divide by 113 EP016 Programmable Divider Waveforms

Applications Information (continued)

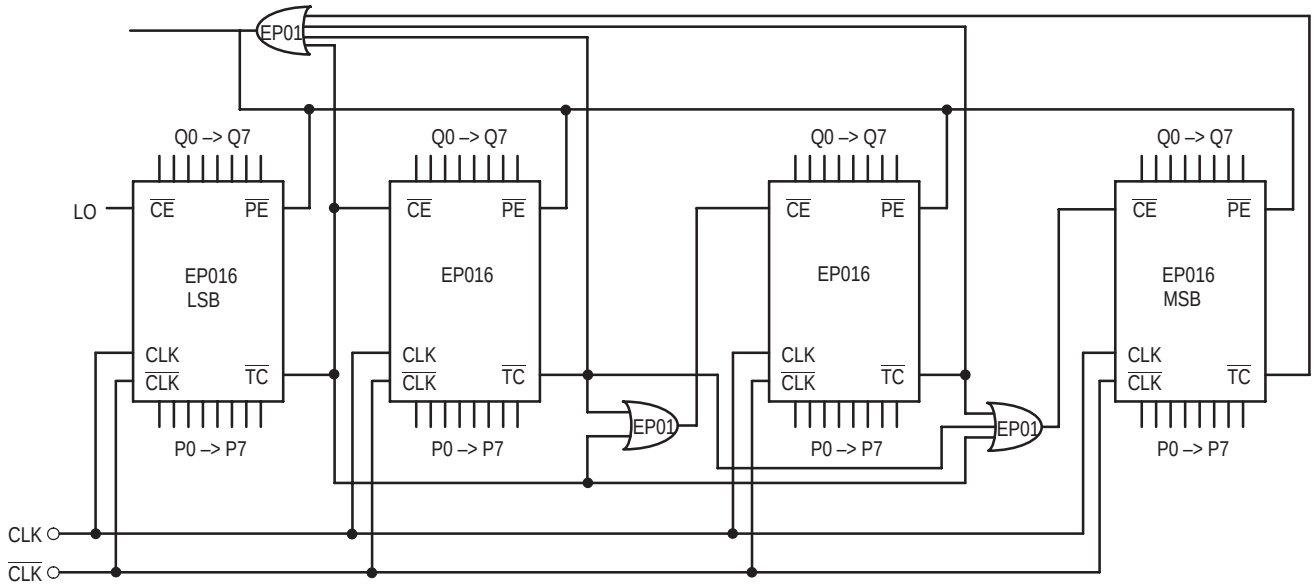


Figure 5. 32-Bit Cascaded EP016 Programmable Divider

Figure 5 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant EP016 must also feed the $\overline{CE}$ input of the most significant EP016. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Figure 6 shows a typical block diagram of a 32–bit divider chain using $\overline{COUT}$ and no external components. This may cause a reduced maximum frequency due to internal gate delays.

Maximizing EP016 Count Frequency

The EP016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

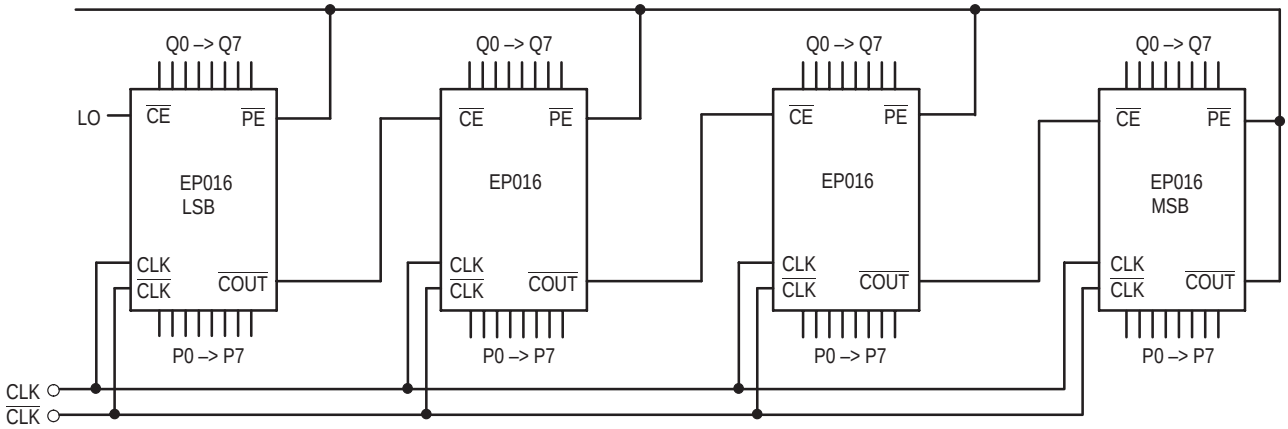


Figure 6. 32-Bit Cascaded EP016 Programmable Divider without external gates

MC100LVEP14

Product Preview

Low-Voltage 1:5 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver

The MC100LVEP14 is a low skew 1–to–5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The LVECL/LVPECL input signals can be either differential or single–ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP14 is operating under LVPECL conditions.

The LVEP14 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all five pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVEP14, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP14 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a $V_{CC} \geq 3.0V$ in LVPECL mode, or $V_{EE} \leq -3.0V$ in LVECL mode. Designers can take advantage of the LVEP14's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using LVPECL, designers should refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 25ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- 400ps Typical Propagation Delay
- High Bandwidth to 1.5 Ghz Typical
- LVPECL and HSTL mode: +2.375V to +3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- 75kΩ Internal Input Pulldown Resistors on CLKs, Pull up & Pulldown resistors on $\overline{CLK}$s
- ESD Protection: >2KV HBM; >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 357 devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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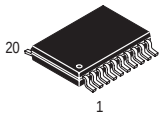
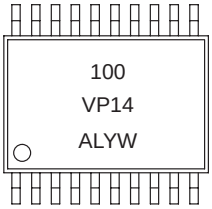


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP14DT	TSSOP	75 Units/Tray
MC100LVEP14DTR2	TSSOP	2500 Tape & Reel

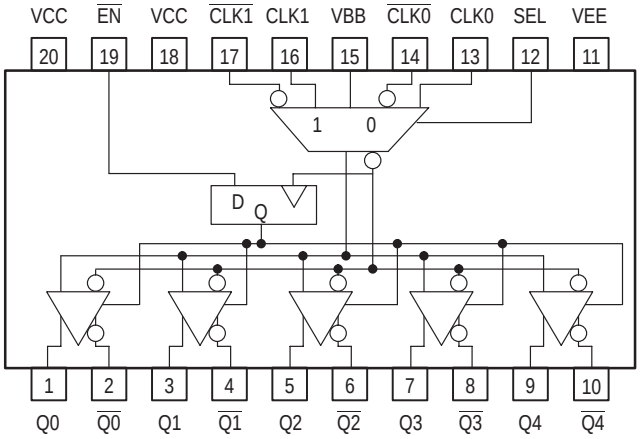


Figure 1. 20–Lead TSSOP and Logic Diagram
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
CLK0, $\overline{\text{CLK0}}$	LVECL/LVPECL/HSTL CLK Input
CLK1, $\overline{\text{CLK1}}$	LVECL/LVPECL/HSTL CLK Input
Q0:4, $\overline{\text{Q0:4}}$	LVECL/LVPECL Outputs
CLK_SEL	LVECL/LVPECL Active Clock Select Input
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

FUNCTION TABLE

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

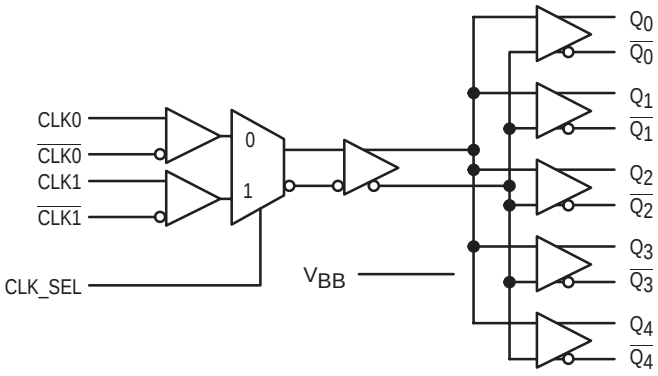


Figure 2. Logic Symbol

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	30 to 35	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Note 1.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV
V_{IH}	Input HIGH Voltage	–1165		–0880	–1165		–0880	–1165		–0880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Reference Voltage (Note 3.)	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \leq$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\mathfrak{X}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 6.)		100			100			100		mA

6. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 11.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 7.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 8.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Reference Voltage (Note 9.)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	µA

7. V_{CCmin} to V_{CCmax}.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Single ended input operation is limited $V_{CC} \geq$ 3.0V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
11. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 15.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 12.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 13.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 13.)	555	680	805	555	680	805	555	680	805	mV
V_{IH}	Input HIGH Voltage	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input LOW Voltage	690		1025	690		1025	690		1025	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	µA

12. V_{CCmin} to V_{CCmax}.
13. All loading with 50 ohms to V_{EE}.
14. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
15. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5(+0.125, –1.3)V)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
$f_{maxLVPECL}$	Maximum Input Frequency for LVECL and LVPECL		1.5			1.5			1.5		GHz
$f_{maxHSTL}$	Maximum Input Frequency for HSTL		250			250			250		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)					 400 400					ps
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)		25 100			25 100			25 100		ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)		180			180			180		ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions.

MC100LVEP111

Product Preview

Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

The MC100LVEP111 is a low skew 1–to–10 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The LVECL/LVPECL input signals can be either differential or single–ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP111 is operating under LVPECL conditions.

The LVEP111 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all ten pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

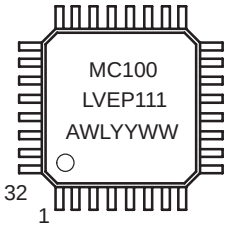
The MC100LVEP111, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a $V_{CC} \geq 3.0V$ in LVPECL mode, or $V_{EE} \leq -3.0V$ in LVECL mode. Designers can take advantage of the LVEP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using LVPECL, designers should refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 25ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- 400ps Typical Propagation Delay
- High Bandwidth to 1.5 Ghz Typical
- LVPECL and HSTL mode: +2.375V to +3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- 75kΩ Internal Input Pulldown Resistors on CLKs, Pull up & Pulldown resistors on $\overline{CLK}$s
- ESD Protection: >2KV HBM; >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 602 devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP111FA	TQFP	250 Units/Tray
MC100LVEP111FAR2	TQFP	2000 Tape & Reel

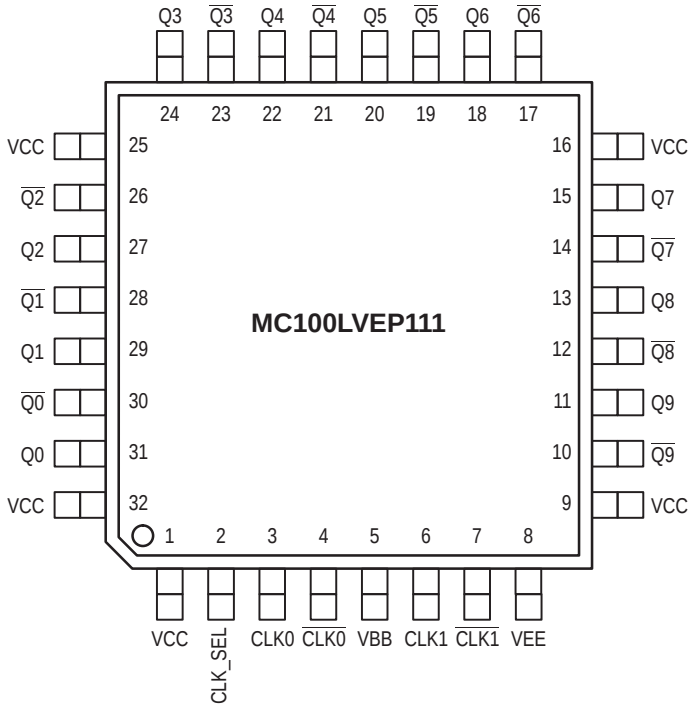


Figure 1. 32–Lead TQFP Pinout
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
CLK0, $\overline{\text{CLK0}}$	LVECL/LVPECL/HSTL CLK Input
CLK1, $\overline{\text{CLK1}}$	LVECL/LVPECL/HSTL CLK Input
Q0:9, $\overline{\text{Q0:9}}$	LVECL/LVPECL Outputs
CLK_SEL	LVECL/LVPECL Active Clock Select Input
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

FUNCTION TABLE

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

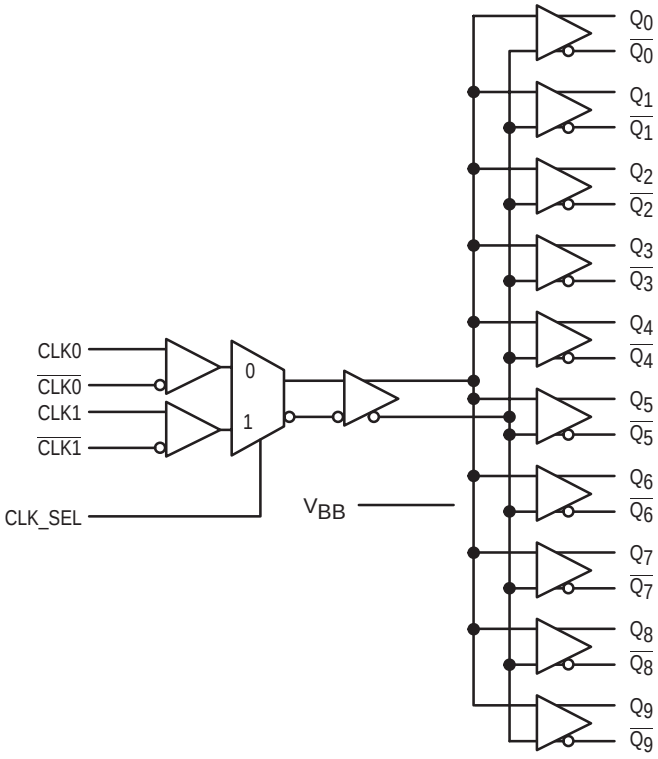


Figure 2. Logic Symbol

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Note 1.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV
V_{IH}	Input HIGH Voltage	–1165		–0880	–1165		–0880	–1165		–0880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Reference Voltage (Note 3.)	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \leq$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\mathfrak{X}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 6.)		100			100			100		mA

6. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 11.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 7.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 8.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Reference Voltage (Note 9.)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	µA

7. V_{CCmin} to V_{CCmax}.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Single ended input operation is limited $V_{CC} \geq$ 3.0V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
11. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 15.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 12.)		100			100			100		mA
V_{OH}	Output HIGH Voltage (Note 13.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 13.)	555	680	805	555	680	805	555	680	805	mV
V_{IH}	Input HIGH Voltage	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input LOW Voltage	690		1025	690		1025	690		1025	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	µA

12. V_{CCmin} to V_{CCmax}.
13. All loading with 50 ohms to V_{EE}.
14. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
15. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5(+0.125, –1.3)V)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
$f_{maxLVPECL}$	Maximum Input Frequency for LVECL and LVPECL		1.5			1.5			1.5		GHz
$f_{maxHSTL}$	Maximum Input Frequency for HSTL		250			250			250		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)					 400 400					ps
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)		25 100			25 100			25 100		ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)		180			180			180		ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions.

MC100LVEP210

Product Preview

Low-Voltage 1:5 Dual Diff. LVECL/LVPECL/LVEPECL/HSTL Clock Driver

The MC100LVEP210 is a low skew 1–to–5 dual differential driver, designed with clock distribution in mind. The LVECL/LVPECL input signals can be either differential or single–ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs. HSTL inputs can be used when the EP210 is operating in LVPECL mode.

The LVEP210 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all ten pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVEP210, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP210 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a VCC ≥ 3.0V in PECL mode, or VEE ≤ –3.0V in ECL mode.

Designers can take advantage of the LVEP210's performance to distribute low skew clocks across the backplane or the board. In a LVPECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 35ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- 475ps Typical Propagation Delay
- High Bandwidth to 1.5GHz Typical
- LVPECL and HSTL mode: 2.375V to 3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Pullup and Pulldown on $\overline{CLK}$
- ESD Protection: >2KV HBM, >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 461 devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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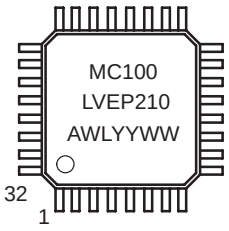
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP210FA	TQFP	250 Units/Tray
MC100LVEP210FAR2	TQFP	2000 Tape & Reel

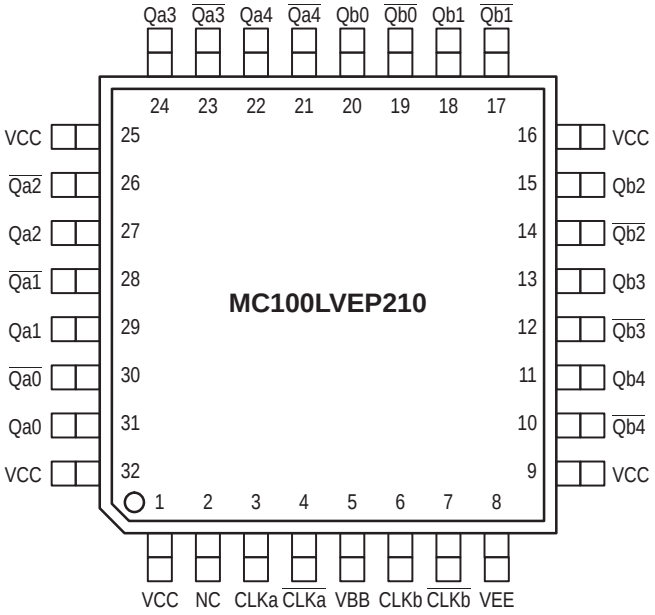


Figure 1. 32–Lead TQFP Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION	
PIN	**FUNCTION**
CLKn/$\overline{\text{CLKn}}$	LVECL/LVPECL/HSTL CLK Inputs
Qn0:4/$\overline{\text{Qn0:4}}$	LVECL/LVPECL Outputs
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

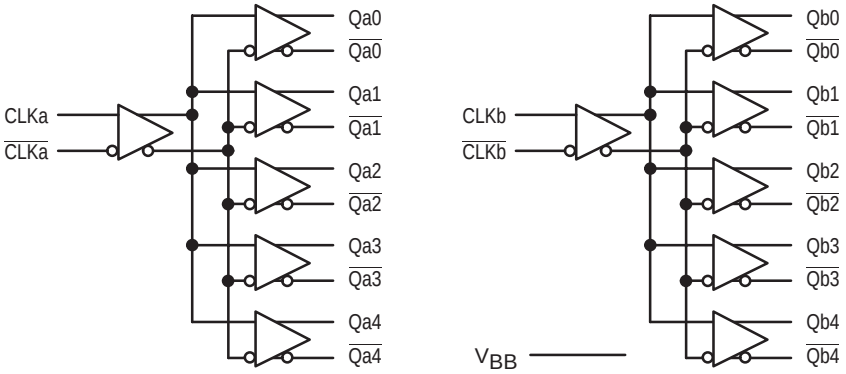


Figure 2. Logic Symbol

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					70					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference (Note 3.)	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \le$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 10.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 6.)					70					mA
V_{OH}	Output HIGH Voltage (Note 7.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 7.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference (Note 8.)	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 9.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

6. V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V, all other pins floating.
7. All loading with 50 ohms to V_{CC}–2.0 volts.
8. Single ended input operation is limited $V_{CC} \ge$ –3.0V in PECL mode.
9. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
10. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 14.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 11.)					70					mA
V_{OH}	Output HIGH Voltage (Note 12.)	1365	1440	1615	1430	1555	1680	1490	1615	1740	mV
V_{OL}	Output LOW Voltage (Note 12.)	565	690	815	630	755	880	690	815	940	mV
V_{IH}	Input HIGH Voltage Single Ended	1290		1615	1355		1680	1415		1740	mV
V_{IL}	Input LOW Voltage Single Ended	565		890	630		955	690		1015	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 13.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

11. V_{CC} = 2.5V, V_{EE} = 0V, all other pins floating.
12. All loading with 50 ohms to V_{EE}.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
14. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\mathfrak{X}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 15.)		100			100			100		mA

15. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5V to –3.8V) or (V_{CC} = 2.5V to 3.8V; V_{EE} = 0V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{maxLVPECL}$	Maximum Toggle Frequency for LVECL and LVPECL (Note 16.)					1.5					GHz
$f_{maxHSTL}$	Maximum Toggle Frequency for HSTL (Note 16.)					250					MHz
t_{PLH}, t_{PHL}	Propagation Delay Differential					475					ps
t_{SKEW}	Within Device Skew Duty Cycle Skew (Note 17.)		TBD TBD			35 100			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)					180 180					ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions of similar paths through a device. Duty cycle skew is defined only for differential operation when the delays are measured from the crosspoint of the inputs to the crosspoint of the outputs.

MC10EPT20

LVTTL/LVCMOS to Differential LVPECL Translator

The MC10EPT20 is a LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package and the single gate of the EPT20 makes it ideal for those applications where space, performance, and low power are at a premium.

- 390ps Typical Propagation Delay
- High Bandwidth to 1.0 GHz Typical
- Differential LVPECL Outputs
- Small Outline SOIC Package
- PNP LVTTL Inputs for Minimal Loading
- V_{CC} Range of 3.0V to 3.6V
- ESD Protection: >1.5KV HBM, >200V MM
- Q Output will default HIGH with inputs open
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 150 devices

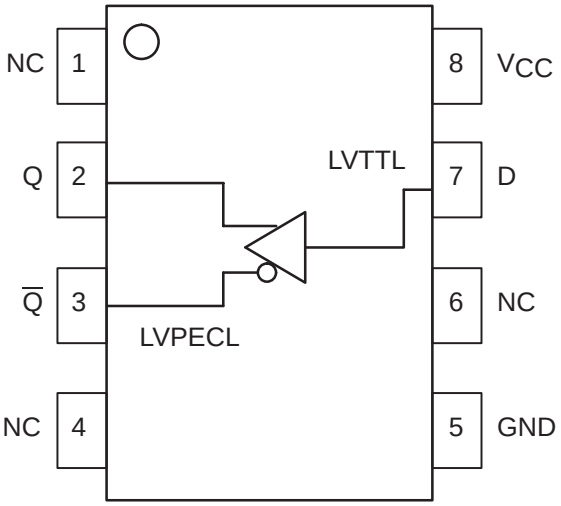


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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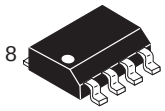

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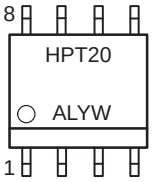
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q, $\overline{Q}$	Differential LVPECL Outputs
D	LVTTL Input
V_{CC}	Positive Supply
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC10EPT20D	SOIC	98 Units/Rail
MC10EPT20DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply	6.0 to 0	VDC
V_I	Input Voltage (V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

LVTTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±0.3V; GND = 0V; T_A = –40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current (V_{in} = 2.7V)			20	μA
I_{IHH}	Input HIGH Current MAX (V_{in} = 6.0V)			100	μA
I_{IL}	Input LOW Current (V_{in} = 0.5V)			–0.6	mA
V_{IK}	Input Clamp Voltage (I_{in} = –18mA)			–1.2	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

LVPECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
ICC	Power Supply Current HIGH (Note 1.)	15	23	31	15	23	31	15	23	31	mA
V_{OH}	Output HIGH Voltage (Note 3.)	2165	2310	2415	2230	2355	2480	2290	2375	2540	mV
V_{OL}	Output LOW Voltage (Note 3.)	1365	1550	1615	1430	1570	1680	1490	1580	1740	mV

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 3.3V, GND = 0V, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)		1000			1000			1000		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	150	350	600	150	370	600	150	380	600	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times (20% – 80%) — Q, $\overline{Q}$	50	100	180	60	120	200	70	140	220	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

MC100EPT21

Differential LVPECL to LVTTL Translator

The MC100EPT21 is a Differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The VBB output allows the EPT21 to also be used in a single–ended input mode. In this mode the VBB output is tied to the $\overline{D0}$ input for a non–inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01μF capacitator.

- 1.4ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1500V HBM, >100V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 81 devices

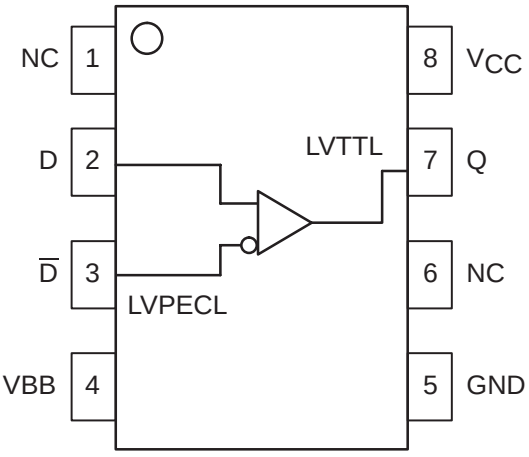


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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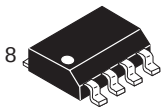

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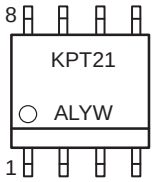
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q	LVTTL Output
D, $\overline{D}$	Differential LVPECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT21D	SOIC	98 Units/Rail
MC100EPT21DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (GND = 0V)	0 to 3.8	VDC
V_I	Input Voltage (GND = 0V, V_I not more positive than V_{CC})	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	5.0	12	20	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	8.0	18	26	mA
V_{IH}	Input HIGH Voltage (V_{CC} = 3.3) (Note 1.)	2135		2420	mV
V_{IL}	Input LOW Voltage (V_{CC} = 3.3) (Note 1.)	1490		1825	mV
I_{IH}	Input HIGH Current			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	µA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 2.)	2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 2.)			0.5	V
I_{OS}	Output Short Circuit Current	–130		–80	mA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V
V_{BB}	Output Voltage Reference		2.0		V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC}.
2. All loading with 500 ohms to GND, CL = 20pF.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)	275	350		275	350		275	350		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	1000 1000	1450 1400	1800 1800	1000 1000	1450 1400	1800 1800	1000 1000	1450 1400	1900 1900	ps
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V – 2.0V) Q, $\overline{Q}$	330	500	900	330	500	900	330	500	900	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
5. Skews are measured between outputs under identical transitions.

MC100EPT22

Dual LVTTL/LVCMOS to Differential LVPECL Translator

The MC100EPT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package and the single gate of the EPT22 makes it ideal for those applications where space, performance, and low power are at a premium. Because the mature MOSAIC 5 process is used, low cost and high speed can be added to the list of features.

- 420ps Typical Propagation Delay
- Differential LVPECL Outputs
- Small Outline SOIC Package
- PNP LVTTL Inputs for Minimal Loading
- Flow Through Pinouts
- Q Output will default HIGH with inputs open
- ESD Protection: 4.0 KV HBM, 200 V MM
- Maximum Frequency > 1.1 GHz
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 164 devices

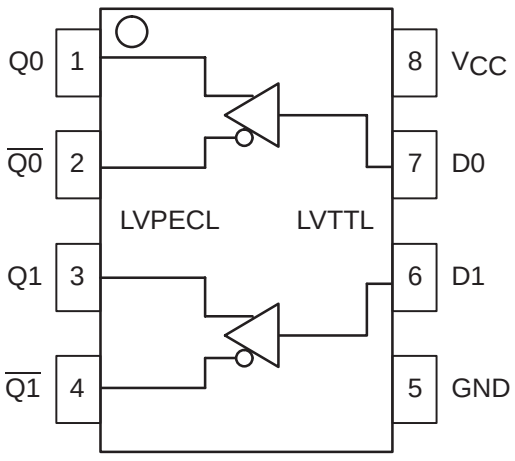


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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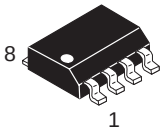

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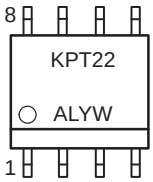
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	Diff. LVPECL Outputs
D0, D1	LVTTL Inputs
V_{CC}	Positive Supply
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT22D	SOIC	98 Units/Rail
MC100EPT22DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply	6.0 to 0	VDC
V_I	Input Voltage (V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

LVTTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±0.3V; GND = 0V; T_A = –40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current (V_{in} = 2.7V)			20	μA
I_{IHH}	Input HIGH Current MAX (V_{in} = 6.0V)			100	μA
I_{IL}	Input LOW Current (V_{in} = 0.5V)			–0.6	mA
V_{IK}	Input Clamp Voltage (I_{in} = –18mA)			–1.0	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

LVPECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, GND = 0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
ICC	Power Supply Current HIGH (Note 1.)	32	43	55	35	45	60	37	46	62	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2100	2240	2400	2100	2280	2400	2100	2350	2400	mV
V_{OL}	Output LOW Voltage (Note 2.)	1350	1490	1600	1350	1555	1600	1350	1550	1600	mV

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 3.3V, GND = 0V, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)	0.8	1.1		0.8	1.1		0.8	1.1		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	250	400	650	250	420	675	300	500	700	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r & t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$	50	110	200	60	120	220	70	140	250	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

MC100EPT23

Dual Differential LVPECL to LVTTL Translator

The MC100EPT23 is a dual differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package and the dual gate design of the EPT23 makes it ideal for applications which require the translation of a clock and a data signal.

The EPT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the EPT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100EPT23 can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3V.

- 1.5ns Typical Propagation Delay
- Minimum Operating Frequency > 275MHz
- Differential LVPECL Inputs
- Small Outline SOIC Package
- 24mA LVTTL Outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1.2KV HBM, >150V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 91 devices

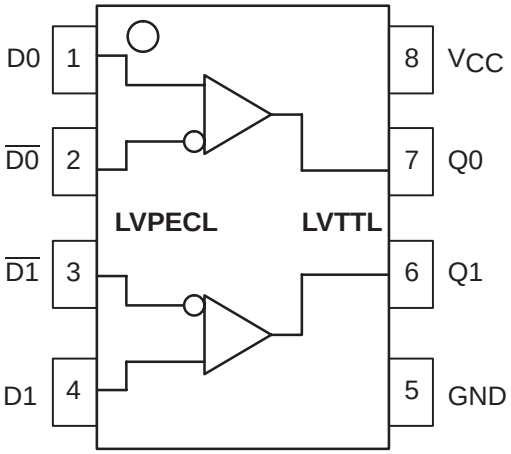


Figure 1. 8–Lead Pinout and Logic Diagram

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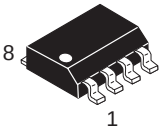

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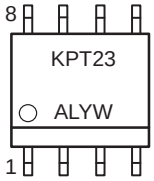
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q0, Q1	LVTTL Outputs
D0, D1, $\overline{D0}$, $\overline{D1}$	Differential LVPECL Inputs
V_{CC}	Positive Supply
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT23D	SOIC	98 Units/Rail
MC100EPT23DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (GND = 0V)	0 to 3.8	VDC
V_I	Input Voltage (GND = 0V, V_I not more positive than V_{CC})	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	26	33	mA
V_{IH}	Input HIGH Voltage (V_{CC} = 3.3) (Note 1.)	2135		2420	mV
V_{IL}	Input LOW Voltage (V_{CC} = 3.3) (Note 1.)	1490		1825	mV
I_{IH}	Input HIGH Current			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	µA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 2.)	2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 2.)			0.5	V
I_{OS}	Output Short Circuit Current	–180		–50	mA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC}.
2. All loading with 500 ohms to GND, CL = 20pF.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)	275	350		275	350		275	350		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (Note 5.)	1.2 1.2	1.5 1.5	1.8 1.8	1.2 1.2	1.5 1.5	1.8 1.8	1.3 1.2	1.7 1.5	2.2 1.8	ns
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 6.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential) (Note 7.)	100	800	1200	100	800	1200	100	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V – 2.0V) Q, $\overline{Q}$	330	600	900	330	600	900	330	650	900	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
5. Reference (V_{CC} = 3.3V ± 5%; GND = 0V)
6. Skews are measured between outputs under identical conditions.
7. 200mV input guarantees full logic swing at the output.

MC100EPT24

LVTTL/LVCMOS to Differential LVECL Translator

The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a –3.3V, +3.3V and ground are required. The small outline 8–lead SOIC package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

The EPT24 is available in the 100E standard and is compatible with ECL 100K logic levels.

- 350ps Typical Propagation Delay
- Maximum Frequency > 1.0GHz
- Differential ECL Outputs
- Small Outline SOIC Package
- PNP LVTTL Inputs for Minimal Loading
- Flow Through Pinouts
- Q Output will default HIGH with inputs open
- ESD Protection: 4000 KV HBM, 200 V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 181 devices

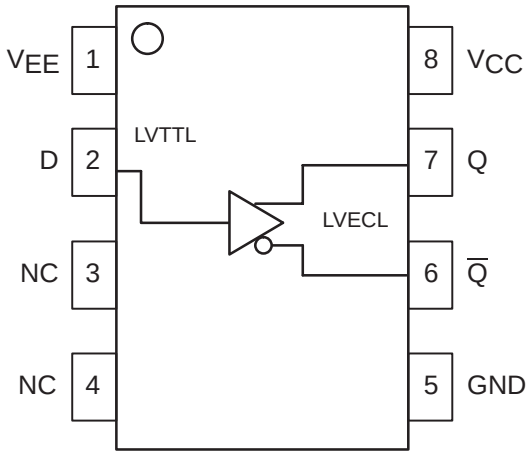


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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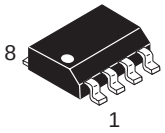

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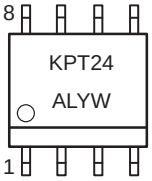
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q, $\overline{Q}$	Differential LVECL Outputs
D	LVTTL Input
V_{CC}	Positive Supply
GND	Ground
V_{EE}	Negative Supply

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT24D	SOIC	98 Units/Rail
MC100EPT24DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–3.8 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	3.8 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–3.8 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	3.8 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

LVTTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±0.3V; GND = 0V; T_A = –40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current (V_{in} = 2.7V)			20	μA
I_{IHH}	Input HIGH Current MAX (V_{in} = 6.0V)			100	μA
I_{IL}	Input LOW Current (V_{in} = 0.5V)			–0.6	mA
V_{IK}	Input Clamp Voltage (I_{in} = –18mA)			–1.2	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

LVECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; V_{EE} = –3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 1.)	-1135	–1020	-885	-1135	–1020	-885	-1135	–1030	-885	mV
V_{OL}	Output LOW Voltage (Note 1.)	-1935	–1750	-1685	-1935	–1770	-1685	-1925	–1790	-1685	mV
I_{CC}	Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	mA
I_{EE}	Power Supply Current	20	30	38	20	30	38	20	30	38	mA

1. Output levels will vary 1:1 with GND; Outputs loaded through 50Ω to GND – 2.0V.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; V_{EE} = –3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 2.)	1.0			1.0			1.0			GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (Note 3.)	300	500	800	300	530	800	300	560	800	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	70	125	170	80	130	180	100	150	200	ps

2. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
3. TTL input of 0V to 3V.

MC100EPT25

Product Preview

Differential LVECL/ECL to LVTTL Translator

The MC100EPT25 is a Differential LVECL/ECL to LVTTL translator. This device requires +3.3V, –3.3V to –5.2V, and ground. The small outline 8–lead SOIC package and the single gate of the EPT25 make it ideal for applications which require the translation of a clock or data signal.

The VBB output allows the EPT25 to also be used in a single–ended input mode. In this mode the VBB output is tied to the D input for a non–inverting buffer or the $\overline{D}$ input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01mF capacitator.

- 1.5ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVECL/ECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >4000V HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 111 devices

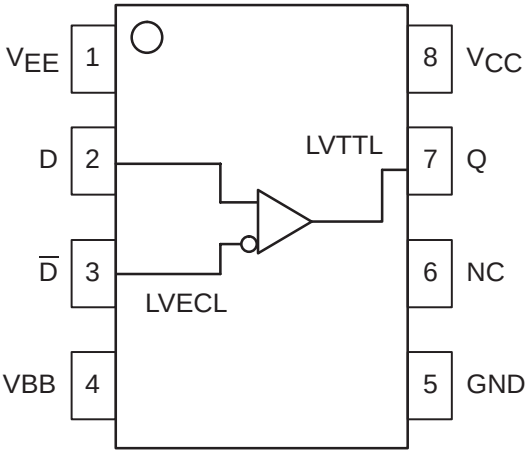


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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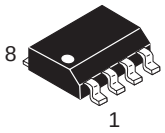

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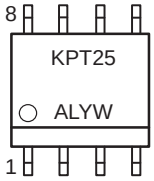
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q	LVTTL Output
D, $\overline{D}$	Differential LVECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
V_{EE}	Negative Supply

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT25D	SOIC	98 Units/Rail
MC100EPT25DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (Referenced to GND, V_{EE} = –3.3V)	0 to 3.8	VDC
V_{EE}	Power Supply (Referenced to GND, V_{CC} = +3.3V)	–6.0 to 0	VDC
V_I	Input Voltage (V_I not more positive than GND)	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = +3.3V; V_{EE} = –5.5V to –3.0V, GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)					20					mA
V_{IH}	Input HIGH Voltage Single Ended (Note 4.)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage Single Ended (Note 4.)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. (V_{CC} = +3.3V, GND = 0V, V_{EE} = –3.3V), all other pins floating.
2. All loading with 500 ohms to GND, C_L = 20pF.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; V_{EE} = –3.3V ± 0.3V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)		12		mA
I_{CCL}	Power Supply Current (Outputs set to LOW)		18		mA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 5.)	2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 5.)			0.5	V
I_{OS}	Output Short Circuit Current	–130		–80	mA
V_{BB}	Output Voltage Reference		–1410		mV

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. All loading with 500 ohms to GND, CL = 20pF.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	275			275			275			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential					1.5					ns
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 6.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential) (Note 7.)	100	800	1200	100	800	1200	100	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (0.8V – 2.0V)					600					ps

6. Skews are measured between outputs under identical conditions.
7. 200mV input guarantees full logic swing at the output.

MC100EPT26

1:2 Fanout Differential LVPECL to LVTTL Translator

The MC100EPT26 is a 1:2 Fanout Differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The VBB output allows the EPT26 to be used in a single–ended input mode. In this mode the VBB output is tied to the $\overline{D0}$ input for a non–inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01μF capacitator.

- 1.4ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flowthrough Pinouts
- ESD Protection: >2KV HBM, >100V MM
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Outputs will default LOW with inputs open or at V_{EE}
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 117 devices

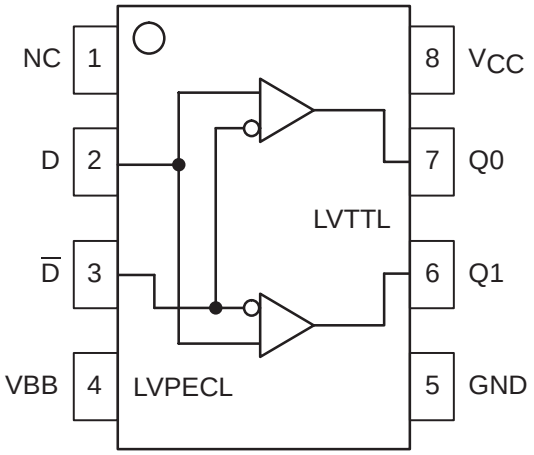


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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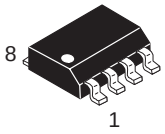

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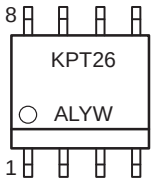
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q0, Q1	LVTTL Outputs
D, $\overline{D}$	Differential LVPECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Reference Voltage
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT26D	SOIC	98 Units/Rail
MC100EPT26DR2	SOIC	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (GND = 0V)	0 to 3.8	VDC
V_I	Input Voltage (GND = 0V, V_I not more positive than V_{CC})	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	20	18	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	28	35	mA
V_{IH}	Input HIGH Voltage (V_{CC} = 3.3) (Note 1.)	2135		2420	mV
V_{IL}	Input LOW Voltage (V_{CC} = 3.3) (Note 1.)	1490		1825	mV
I_{IH}	Input HIGH Current			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	µA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 2.)	2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 2.)			0.5	V
I_{OS}	Output Short Circuit Current	–50		–150	mA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V
V_{BB}	Output Voltage Reference		2.0		V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC}.
2. All loading with 500 ohms to GND, CL = 20pF.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)	275			275			275			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	500	1500	2500	500	1500	2500	500	1500	2500	ps
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V – 2.0V) Q, $\overline{Q}$	330	500	900	330	500	900	330	550	950	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
5. Skews are measured between outputs under identical transitions.

Application Notes

The ECL Translator Guide

ECL • TTL • PECL • LVECL • LVPECL • CMOS • LVTTL

How To Make Them Talk To Each Other

Prepared by
Paul Shockman, Paul Hunt
ON Semiconductor Logic Applications Engineering

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

Are You Designing with Different I/O Levels?

This document guides you to the appropriate interface.

For interfacing between ECL devices and the TTL / CMOS world discrete interfaces could be used. But the switching points are usually not controlled and may vary with temperature, device variation, or supply voltage. This results in duty cycle variation. To avoid this signal quality uncertainty translating devices with controlled switching levels and specified propagation delays and skews are available.

Translation between ECL signals off different power supplies might be done by capacitive coupling. But this is only possible for clock signals or RZ coded signals. For this reason special translators are available.

If you are looking for interfaces between LVDS and ECL, please see the application note AN1568/D “Interfacing Between LVDS and ECL”.

You will find the right device for your application in the translator table on page 113. The tables give you additional information on the bit–width and the databook location.

Translators from TTL–World to ECL–World

TTL to ECL Translators (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
1	MC10/100ELT24	TTL to Differential ECL	DL140
4	MC10124	Quad TTL to MECL	DL122
4	MC10H124	Quad TTL to MECL with TTL Strobe	DL122
4	MC10H424	Quad TTL to PECL with ECL Strobe	DL122
6	MC10/100H604	Registered Hex TTL/ECL	DL122
9	MC10/100H600	9 Bit TTL/ECL	DL122
9	MC10/100H602	9 Bit Latch TTL/ECL	DL122

TTL/ECL Transceiver (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
4	MC10/100H680	4 Bit Differential ECL Bus/TTL Bus Transceiver with Latches	DL122
6	MC10/100H681	Hex Differential ECL/TTL Transceiver with Latches	DL122

TTL to PECL (Single Supply +5 V)

Width	Device	Function	Databook
1	MC10/100ELT20	TTL to Differential PECL	DL140
2	MC10/100ELT22	Dual TTL to Differential PECL	DL140
4	MC10H351	Quad TTL/NMOS to PECL	DL122
6	MC10/100H606	Registered Hex TTL/PECL	DL122

LVTTL to LVPECL (Single Supply +3.3 V)

Width	Device	Function	Databook
2	MC100LVELT22	Dual LVPECL to LVTTL	onsemi.com
1	MC10EPT20	LVPECL to LVTTL	BR1513
2	MC100EPT22	Dual LVPECL to LVTTL	BR1513

Translators from ECL–World to TTL–World

ECL to TTL (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
1	MC10/100ELT25	Differential ECL to TTL	DL140
4	MC10125	Quad MECL to TTL	DL122
4	MC10H125	Quad MECL to TTL	DL122
4	MC10/100H660	4 Bit ECL TTL Load Reducing DRAM Driver	DL122
6	MC10/100H605	Registered Hex ECL/TTL	DL122
9	MC10/100H601	9 Bit ECL/TTL	DL122
9	MC10/100H603	9 Bit Latch ECL/TTL	DL122

PECL to TTL (Single Supply +5 V)

Width	Device	Function	Databook
1	MC10/100ELT21	Differential PECL to TTL	DL140
2	MC100ELT23	Dual Differential PECL to TTL	DL140
4	MC10H350	Differential PECL to TTL	DL122
6	MC10/100H607	Registered Hex PECL/TTL	DL122

LVPECL to LVTTL (Single Supply +3.3 V)

Width	Device	Function	Databook
1	MC100EPT21	Differential LVPECL to LVTTL	BR1513
2	MC100EPT23	Dual Differential LVPECL to LVTTL	BR1513
2	MC100LVELT23	Dual Differential LVPECL to LVTTL	onsemi.com
2	MC100EPT26	1:2 Differential LVPECL to TTL	BR1513

LVTTL to ECL/LVECL (Dual Supply +3.3 V, –3.3V to –5V)

Width	Device	Function	Databook
1	MC100EPT24	LVTTL to Differential LVECL	BR1513

ECL/LVECL to LVTTL (Dual Supply +3.3 V, –3.3V to –5V)

Width	Device	Function	Databook
1	MC100EPT25	Differential LVECL to LVTTL	BR1513

PECL–TTL and TTL–PECL (Single Supply +5 V)

Width	Device	Function	Databook
1+1	MC10/100ELT28*	TTL to Differential PECL + Differential PECL to TTL	DL140

CMOS to PECL Interfacing

	Width	Device	Function	Databook
CMOS to PECL (Single +5 V)	4	MC10H352	Quad CMOS to PECL	DL122

Different Supplied ECL

	Width	Device	Function	Databook
LVECL to PECL (−3.3 V to +5 V)	3	MC100EL90	Triple ECL to PECL	DL140
LVECL to LVPECL (−3.3 V to +3.3 V)	3	MC100LVEL90	Triple ECL to LVPECL	DL140
LVPECL to ECL (−3.3 V to MECL)	3	MC100EL91	Triple LVPECL to ECL	DL140
LVPECL to LVECL (+3.3 V to −3.3 V)	3	MC100LVEL91	Triple LVPECL to LVECL	DL140
PECL to ECL (+5 V to MECL)	3	MC100EL91	Triple PECL to LVECL	DL140
PECL to LVECL (5 V to −3.3 V)	3	MC100EL91	Triple PECL to LVPECL	DL140
PECL to LVPECL (5 V to +3.3 V)	3	MC100LVEL92	Triple PECL to LVPECL	DL140
ECL to PECL (MECL to +5 V)	3	MC100EL90	Triple ECL to LVPECL	DL140
ECL to LVPECL	3	MC100LVEL90	Triple ECL to LVPECL	DL140

Translator Table

From/To	TTL VCC = +5V	ECL VEE= –4.5/–5.2V	PECL VCC = +5V	LVTTL VCC = +3.3V	LVECL VEE = –3.3V	LVPECL VCC = +3.3V	CMOS VDD = +5V
TTL	standard connection	124 H424 H124 H600 H602 H604 H680* H681* ELT24	H351 H606 ELT20 ELT22 ELT28*	(Use +5V input tolerant devices)	EL91	EPT20, EPT22, or LVELT22 With VIH limited to VCC = 3.3V	Pull up resistor
ECL VEE = –4.5/–5.2V	125 H125 H601 H603 H605 H660 H680* H681* ELT25	standard connection	EL90	EPT25	standard connection	LVEL90	ECL/TTL Translator to HCT or ACT input
PECL VCC = +5V	H350 H607 ELT21 ELT23 ELT28*	EL91	standard connection	LVEL92 + LVELT23, EPT23, or EPT21	EL91	LVEL92	PECL/TTL Translator to HCT or ACT input
LVTTL VCC = 3.3V	Direct connection, as DC levels are identical	EPT24	(EPT20, EPT22, or LVELT22) + 5V ECL line receiver, e.g.(EL17) EL90	standard connection	EPT24	EPT20 EPT22 LVELT22	Pull up resistor
LVECL VEE = –3.3V	ELT25	Standard connection, as DC levels are identical	EL90	EPT25	standard connection	LVEL90	ECL/TTL Translator to HCT or ACT input (–5V required)
LVPECL VCC = +3.3V	ELT21 ELT23 ELT28*	EL91	ECL line receiver, e.g. EL17	EPT21 EPT23 LVELT23 EPT26	LVEL91	Direct connection	Direct connection
CMOS VDD = +5V	Direct connection	H352 + EL90	H352	VIA LCX	H352 + EL90	LCX + LVELT22, EPT20, or EPT22	

*Bidirectional

AND8002/D

ECLinPS Lite™ and ECLinPS Plus™ Device Type and Date Code Guide

Gary Richards, ECL Logic Product Engineering

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

DEVICE TYPE MARKING

This is a summary of ECLinPS Lite and ECLinPS Plus device labeling guidelines.

MC Device Nomenclature:

Standard ECL family abbreviations used are:

ECL = Emitter Coupled Logic
E = ECLinPS,
EL = E–Lite = ECLinPS Lite,
LV = Low Voltage,
T = Translator,
EP = E–Plus = ECLinPS Plus.

These can be used in combination;

ELT = ECLinPS Lite Translator,
EPT = ECLinPS Plus Translator,
LVE = Low Voltage ECLinPS,
LVEL = Low Voltage ECLinPS Lite,
LVELT = Low Voltage ECLinPS Lite Translator.

Device Labeling Example:

MC100LVEL14D
MC = Motorola/ON Semiconductor brand
100 = 100K/100E Voltage and Temperature Compensation
LVEL = Low Voltage ECLinPS Lite,
14 = Function
D = Package Type

Notes:

The combinations: LVET, LVEP, LVEPT are not used.
All “MC” devices follow the same format.

MC Device Markings:

For packages larger than 20–lead SOIC the marking is the same as the device type.

The 16–lead and 20–lead SOIC marking scheme is truncated as follows:

16–Lead SOIC:

Device Nomenclature	Marking
MC10EL15D =	**10EL15**
MC100EL15D =	**100EL15**

20–Lead SOIC:

MC100EL13DW =	**100EL13**
MC100LVEL13DW =	**100LVEL13**

Device marking is most challenging on 8–lead SOIC devices which do not have physical space on small packages for full marking. Because device marking is limited to 5 characters, the E for ECLinPS representation will be dropped as in the case of low voltage and translator functions in ECLinPS Lite and ECLinPS Plus families.

Standard ECL family marking abbreviations:

H = 10, to represent 10H/10E compatible, voltage–compensated only.
K = 100, to represent 100K/100E compatible, voltage and temperature compensated.
L = ECLinPS Lite.
V = LV = Low Voltage
T = Translator.
P = ECLinPS Plus.
PT = EPT = ECLinPS Plus Translator.

8–Lead SOIC:

Device Nomenclature	Marking
MC10EL01D =	**HEL01**
MC100EL01D =	**KEL01**
MC100LVEL11D =	**KVL11**
MC10ELT20D =	**HLT20**
MC100ELT20D =	**KLT20**
MC100LVELT22D =	**KVT22**
MC10EP01D =	**HEP01**
MC100EP01D =	**KEP01**
MC10EPT20D =	**HPT20**
MC100EPT23D =	**KPT23**

PC/XC Device Marking

New Prototype “PC” devices and new pre–production release, pre–reliability “XC” devices:

P = PC
X = XC

The first character is the “PC” or “XC” identifier. For a variety of reasons, the remaining characters have not been standard for different engineering devices. On these devices the date code will be the most important item.

Examples of current markings:

XVT23 = XC100LVELT23D
PEP16 = PC10EP16D
PET23 = PC100EPT23D

DATE CODE MARKING

This is a summary of ECLinPS Lite and ECLinPS Plus Date Code Marking. The intent is to summarize and explain the Date Code Marking for ECLinPS Lite and ECLinPS Plus small SOIC packages only. To properly understand the ECLinPS Lite and ECLinPS Plus family marking, please contact your ON Semiconductor representative, or review the individual device specifications.

Date Code / Alpha Code Marking:

20–Lead SOIC = “AWLYYWW”

“A” – The First character indicates the Assembly Location.
“WL” – The Second & Third characters indicate the Wafer Lot Tracking Code.
“YY” – The Fourth & Fifth characters indicate the Year Assembled.
“WW” – The Sixth & Seventh characters indicate the Work Week Assembled.
100LVEL56 = MC100LVEL56DW

XAA9646
|||||||
X|||||| = ASE Chung–Li (previously Motorola METL) Taiwan. Assy Location.
AA|||| = First Lot Assembled for that Device Type in that (Work Week).
96|| = 1996
46 = WW46

16–Lead SOIC = “AWLYWW”

“A” – The First character indicates the Assembly Location.
“WL” – The Second & Third characters indicate the Wafer Lot Tracking Code.
“Y” – The Fourth character indicates the Year Assembled.
“WW” – The Fifth & Sixth characters indicate the Work Week Assembled.
10EL34 = MC10EL34D

XAA643
||||||
X||||| = ASE Chung–Li (previously Motorola METL) Taiwan. Assy Location.
AA||| = First Lot Assembled for that Device Type in that (Work Week).
6|| = 1996
43 = WW43

Only 4 characters are used on 8–lead SOIC. Therefore, the following abbreviations are used:

8–Lead SOIC Example = “ALYW”

“A” – The First character indicates the location of Assembly Location.
“L” – The Second character indicates the Wafer Lot Tracking Code.
“Y” – The Third character indicate an “ALPHA CODE” of the Year assembled.
“W” – The Fourth character indicate an “ALPHA CODE” of the Work Week assembled.

The “Y” YEAR Alpha Codes are:

A = 1989 First	6 months,	WW01 – WW26
B = 1989 Second	6 months,	WW27 – WW52
C = 1990 First	6 months,	WW01 – WW26
D = 1990 Second	6 months,	WW27 – WW52
E = 1991 First	6 months,	WW01 – WW26
F = 1991 Second	6 months,	WW27 – WW52
G = 1992 First	6 months,	WW01 – WW26
H = 1992 Second	6 months,	WW27 – WW52
I = 1993 First	6 months,	WW01 – WW26
J = 1993 Second	6 months,	WW27 – WW52
K = 1994 First	6 months,	WW01 – WW26
L = 1994 Second	6 months,	WW27 – WW52
M = 1995 First	6 months,	WW01 – WW26
N = 1995 Second	6 months,	WW27 – WW52
O = 1996 First	6 months,	WW01 – WW26
P = 1996 Second	6 months,	WW27 – WW52
Q = 1997 First	6 months,	WW01 – WW26
R = 1997 Second	6 months,	WW27 – WW52
S = 1998 First	6 months,	WW01 – WW26
T = 1998 Second	6 months,	WW27 – WW52
U = 1999 First	6 months,	WW01 – WW26
V = 1999 Second	6 months,	WW27 – WW52
W = 2000 First	6 months,	WW01 – WW26
X = 2000 Second	6 months,	WW27 – WW52
Y = 2001 First	6 months,	WW01 – WW26
Z = 2001 Second	6 months,	WW27 – WW52

The “W” Work Week Alpha Codes are:

First 6 months WW01 – WW26	Second 6 months WW27 – WW52	First 6 months WW01 – WW26	Second 6 months WW27 – WW52
A = 01	A = 27	N = 14	N = 40
B = 02	B = 28	O = 15	O = 41
C = 03	C = 29	P = 16	P = 42
D = 04	D = 30	Q = 17	Q = 43
E = 05	E = 31	R = 18	R = 44
F = 06	F = 32	S = 19	S = 45
G = 07	G = 33	T = 20	T = 46
H = 08	H = 34	U = 21	U = 47
I = 09	I = 35	V = 22	V = 48
J = 10	J = 36	W = 23	W = 49
K = 11	K = 37	X = 24	X = 50
L = 12	L = 38	Y = 25	Y = 51
M = 13	M = 39	Z = 26	Z = 52

The date code can be determined from this information as shown in the following example:

```
XANS,
||||
X||| = ASE Chung–Li (previously Motorola METL) Taiwan. Assy Location.
 |||
 A|| = First Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  N| = 1995 Second  6 months, WW27 – WW52
   |
   S = WW45 (Y95 WW45)

XBST,
||||
X||| = ASE Chung–Li (previously Motorola METL) Taiwan. Assy Location.
 |||
 B|| = Second Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  S| = 1998 First  6 months, WW01 – WW26
   |
   T = WW20 (Y98 WW20)
```

Additional Assistance

For additional assistance, please contact your local ON Semiconductor representative. You may also order the High Performance ECL Data Book from the Literature Distribution Center as document DL140/D or the ECLinPS Plus Data Brochure as document BR1513/D. See below for Publication Ordering Information.

Storage and Handling of Drypacked Surface Mounted Devices (SMD)

Prepared by: R. Kampa, D. Hagen, W. Lindsay, and K.C. Brown

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

INTRODUCTION

This information provides ON Semiconductor customers with the necessary storage and handling guidelines to preclude component package cracking during solder reflow procedures.

This document applies to plastic encapsulated SMDs that ON Semiconductor identifies as moisture sensitive and delivers in a drypack. Moisture sensitive SMDs include, but are not limited to small outline J pins (SOJs), plastic leaded chip carriers (PLCCs), quad flat packs (QFPs), plastic quad flat packs (PQFPs), thin quad flat packs (TQFPs), thin small outline packages (TSOPs), small outline integrated circuits (SOICs), and plastic ball grid arrays (PBGAs).

SMD PACKAGE LIMITATIONS

During reflow procedures, moisture absorbed from the atmosphere will vaporize inside an SMD and swell into a vapor dome. The internal stresses exerted by the vapor dome are directly proportional to the amount of moisture absorbed prior to reflow. The pressure from the vapor dome may cause of one or more of the internal package interfaces to delaminate. This pressure may also form cracks in the mold compound and possibly expose the die to the external environment.

Both, die surface delaminating and package cracks, pose potential reliability problems. By following the guidelines herein, ON Semiconductor customers will avoid the occurrence of these problems.

DRYPACK DESCRIPTION

Drypack consists of a moisture vapor barrier bag with a preprinted moisture sensitive warning label, a desiccant, and RH indicator, and a barcode label.

The bag construction consists of a three layer laminate; tyvek or nylon for puncture resistance, aluminum for a moisture barrier, and polyethylene for an airtight seal.

The preprinted warning label identifies the contents as moisture sensitive and outlines the recommended storage and handling requirements and shelf life.

The desiccant packed in each bag will keep the internal humidity level below 20% RH for at least one year, under worst case storage conditions of 40°C and 90% RH.

The RH indicator provides the customer with a simple and efficient means to verify that the internal humidity level remains below 20% RH during storage. NOTE: If the RH indicator reads greater than 20% RH at 23°C ± 5°C immediately upon opening the bag, then the SMDs contained therein must undergo a dry–out procedure (see Dry–Out Procedures) prior to any reflow process.

The barcode label identifies the bag seal date and the qualified moisture sensitivity level of the SMD. An ON Semiconductor Standard Operating Procedure (S.O.P.) specification titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices” defines the requirements for qualifying the moisture sensitivity level of a plastic SMD and meets the intent of JEDEC A112, Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices, and JEDEC A113, Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.

STORAGE REQUIREMENTS AND TIME LIMITS OUT OF DRYPACK

The qualified moisture sensitivity level for each SMD determines the appropriate storage requirements and time limits once out of drypack. Table 1 relates the moisture sensitivity (MS) level to the storage environment and time limits. If these limits are exceeded once the drypack is removed, then the effected SMDs must undergo a dry–out procedure prior to any reflow process.

Table 1.

MS Level	Drypack	Storage TH	Time Out of Drypack
1	No	30°C / 90% RH	Indefinite
2	Yes	30°C / 60% RH	One Year
3	Yes	30°C / 60% RH	168 Hours Max
4	Yes	30°C / 60% RH	72 Hours Max
5	Yes	30°C / 60% RH	24 Hours Max
6	Yes	30°C / 60% RH	6 Hours Max

OPTIONAL STORAGE METHODS OUT OF DRYPACK

If the customer cannot mount the SMDs within the specified time limit, or factory ambient conditions exceed the specified maximum temperature and/or humidity level, then the customer can abate moisture absorption by immediately storing the SMDs at less than 20% RH. Any of the following storage methods may be used.

Store the SMDs in a rigid metal container with a tight fitting lid. Place fresh desiccant (as a minimum, the equivalent of one ON Semiconductor desiccant bag per every 0.8 cubic feet) in the storage container. Desiccant is readily available at any chemical supply house. An RH indicator strip must be kept inside the container to verify that the humidity level remains below 20 percent.

Store the SMDs in a dry nitrogen purge cabinet or container that maintains the humidity level at less than 20 % RH.

For short term storage, SMDs can be resealed in the original drypack bag soon after opening. Bags opened carefully near the seal are easily resealed with either a heat seal or a tight fitting clip. Fresh desiccant may be required in equal proportion to the amount originally shipped with the bag. An RH indicator strip must be kept inside the bag to verify that the humidity level remains below 20% RH.

DRY–OUT PROCEDURES

SMDs that are not handled or stored within specification must undergo one of the following dry–out procedures prior to reflow.

125°C DRY–OUT BAKE

Bake TSOPs at 125°C (± 5°C) for four hours (+1/–0 hour). Bake all other SMDs at 125°C (± 5°C) for eight hours (+1/–0 hour). CAUTION:Do not bake SMDs in shipping trays with a temperature rating of less than 130°C. Do not bake SMDs in plastic tubes or tape and reel (T & R) packaging. Use care in handling SMDs out of their shipping container to maintain lead coplanarity.

40°C DRY–OUT BAKE

Bake TSOPs at 40°C (± 5°C) for 96 hours (± eight hours). Bake all other SMDs at 40°C (± 5°C) for 168 hours (± eight hours). NOTE: This bake is designed for SMDs in plastic tubes or T&R, and is best achieved in a dry nitrogen purge oven. Higher temperatures warp or melt plastic tubes and T&R cover tape separates from carrier tape at 60°C.

ROOM TEMPERATURE DRY–OUT

Store units per Optional Storage Methods for a minimum of 500 hours. This drying method is designed for SMDs in plastic tubes or T&R when a 40°C dry–out bake is not possible or desirable.

NOTE:
The customer must apply the same storage requirements and time limits specified in Storage Requirements to all dried SMDs

SOLDER REFLOW PROFILES

The following guidelines do not necessarily indicate the temperature extremes that can safely be applied to SMDs. In most cases and SMD can withstand higher temperatures than the standard PC board. These guidelines represent good soldering practices that will yield high quality assemblies and minimize rework.

VAPOR PHASE REFLOW

Preheat leads to a nominal temperature of 150°C at a maximum rate of 2°C per second.

Operate the reflow chamber between 215°C and 220°C maximum, with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting pint of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Some vapor phase machines cannot provide preheat, and therefore subject boards and components to rather severe thermal shocks.

INFRARED REFLOW

Preheat leads to a temperature of 100°C minimum and a 140°C maximum rate of 2°C per second.

Generate peak lead temperatures between 205°C minimum and 235°C with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting point of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Peak temperatures can vary greatly across the PC board during IR processes. The variables that contribute to this wide temperature range include the furnace type and the size, mass and relative location of the components on the board. Profiles must be carefully tested to determine the hottest and coolest points on the board. The hottest and coolest points should fall within the recommended temperatures. Thermocouples must be carefully attached directly to the solder joint interface between the package leads and the board with very small amounts of thermally conductive grease or epoxy.

WAVE SOLDER

Preheat leads to a temperature of 100°C minimum and 140°C maximum at a maximum rate of 2°C per second.

Generate a solder wave temperature of 245°C nominal, 265°C maximum, with a nominal dwell time of two to three seconds and a maximum dwell time of five seconds

NOTE:
The wave solder process is suitable for the SOIC, but it is not recommended for PLCC, SOJ, QFP, TSOP, PQFP, TQFP or CQFP because of the high rate of bridging and 0pen solder joints caused by shadowing effects. Thermal shock is much greater if the whole body is immersed in molten solder. Wave solder immersion tests have not been conducted on large PLCC, QFP, PQFP, TQFP and CQFP.

REFERENCE DOCUMENTS

JEDEC Test Method A112, “Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices.” JEDEC Test Method A113, “Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.” ON Semiconductor S.O.P. titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices.”

ECLinPS Plus™ SPICE Modeling Kit

Prepared by
Paul Shockman, Paul Hunt
ON Semiconductor Logic Applications Engineering

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

Objective

The Objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modeling for the current devices of the ECLinPS Plus logic line, On Semiconductor's highest performance ECL family. With packaged gate delays of 160ps and output edge rates as low as 130ps this family defines the state–of–the–art in ECL logic. The ECLinPS Plus line is the newest addition to On Semiconductor's highest performance ECL/PECL family of products. The kit is not intended to provide information necessary to perform circuit level modeling on ECLinPS Plus devices.

Device Input and Output Buffers

Schematic Information

The kit contains all the representative input and output schematics used for the ECLinPS Plus devices available at the writing of this note in Table 2, "Netlist Index." This application note will be modified as new devices are added.

Table 1: Schematics and Netlist Nomenclature

LVCC	3.3V FOR LVPECL AND (0V) FOR LVECL
LVEE	–3.3V FOR LVECL AND (0V) FOR LVPECL
GND	0V
IN	INPUT TO CKT
INB	INPUT BAR OF CKT
Q	TRUE OUTPUT OF CKT
QB	INVERTED OUTPUT OF CKT

Package

A worst case model for various package types is included to improve the accuracy of the system model. The package model represents the parasitic as they are measured on a corner pin, a sizable distance from an AC ground pin. If typical values are desired, reduce the inductance and capacitance parameters of the package model by 20%. The package pin model should be placed on each device input pin connecting to an input model, all device output pins connecting to an output model, and the VCC line. A model can be used at the VEE pin: but is not necessary since the current in the VEE pin is a constant.

Input Buffer

The various input buffer schematics are representing structures currently in use on the existing devices in this family. Some of the structures are special and may only be used for one device. The schematics require the addition of ESD and package models to more accurately model behavior; but are otherwise functionally correct. It is unnecessary to include an ESD or Package model for the VBB pins of the models because VBB is intended as an internal node for most applications. If VBB is modeled as an external node it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit.

Output Buffer

The output buffer schematics and netlists contain the temperature compensation structure, and only the ESD and package models need to be added. Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. The output buffers show differential inputs and outputs. When simulating a single ended output, the termination or load resistor, package model, ESD structure and output emitter follower, of the unused output, may be eliminated to simplify the system model. An output buffer may either be driven with an input buffer's out nodes or driven with an internal level directly. Table 2 supplies the necessary internal driving levels and edges. An output buffer may also be driven Differentially or Single Ended.

Table 2: Internal Driving Levels for an Output Buffer

Mode	Structure	IN (V)	INB (V)	t r /t f (20–80%)	LVCC	LVEE
LVPECL	Differential	VCC–.85 → VCC–1.15	VCC–1.15 → VCC–.85	160ps	+3.3V	0V
	Single Ended	VCC–.85 → VCC–1.15	VCC–1.0	160ps		
LVECL	Differential	VCC–.85 → VCC–1.15	VCC–1.15 → VCC–.85	160ps	0V	–3.3V
	Single Ended	VCC–.85 → VCC–1.15	VCC–1.0	160ps		

SPICE Netlists

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of external node interconnects. This may simplify building individual subcircuit netlists into an interconnected simulation model, i.e. an ”input driving an output” model. The netlist nodal naming conventional is given in Table 3.

Table 3: Global Node Numbering

Node	Number
VCC	100
VEE	200
VBB	300
VCS	400
VCLMP	500

Temperature Compensation Network for 10EP

The output netlists include temperature compensation network circuitry for 100EP style output buffers. The circuit components of the temperature compensation networks are QT1, QT2 and RTC. For simulating 10EP style outputs these components should either be deleted or commented out of the subcircuit netlists. There are four terminals on all transistor models: Emitter, Base, Collector, and Substrate (biased to VEE). It should be noted that all circuits can be used single ended or differentially by replacing INB with VBB for single ended and Visa Versa for differential operation.

SPICE Parameter Information

In addition to the schematics and netlists is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have no parasitic capacitance in the real circuit and none is required in the model. The schematics display the only devices needed in the SPICE netlists.

Modeling Information

The bias drivers for the devices are not detailed since their circuitry would result in a substantial increase of model complexity and simulation time. Instead, these internal reference voltages (VBB , LVCS, Etc.) should be driven with ideal constant voltage sources. Table 4 summarizes the levels required as well as some typical input parameters.

Table 4:

Parameter	Typical	Worst Case
VBB	VCC – 1.295V	VCC – (1.295±50mV)
LVCS	VEE + 0.9	VEE + (0.9V±20mV)
VCS	VEE + 1.3V	VEE + (1.3V±50mV)
VIH	VCC – 0.89V	VCC – (VIHmin, max) Data Sheet
VIL	VCC – 1.75V	VCC – (VILmin, max) Data Sheet
t r /t f	400ps (20–80%)	Use Data Book Specifications

The schematics and SPICE parameters will provide a typical output waveshape that may not represent the worst case situation. There are simple adjustments that can be made to the models allowing output characteristics to simulate conditions at or near the corners of the data book specifications.

1) Adjust the gate current:

To produce the desired rise and fall times output slew rates, adjust collector load resistors to adjust the gates tail current.

2) Adjust the VOH:

To adjust the VOH (and VOL level by the same amount), vary LVCC for the desired level. The output levels will follow mV changes in LVCC at a 1:1 ratio.

3) Adjust the VOL:

To adjust the VOL level independently of the VOH level, the collector load resistance must be increased or decreased. Note that the VOH level will also change slightly due to a IbaseR drop across the collector load resistor or VOL can be changed by varying the gate current through the current source resistor.

Summary

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 1. illustrates a typical situation which can be modeled using the information in this kit.

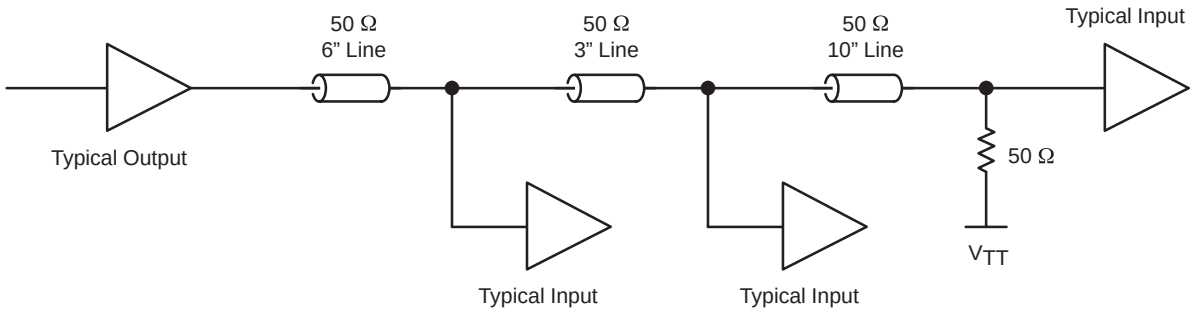


Figure 1. Typical Application for I/O SPICE Modeling Kit

Table 5: Netlist Index

Device	Function	Input	Clock Input	S/R Input	Select Input	Output
EP01	4–Input OR/NOR Gate	INBUF04				OBUF01
EP05	2–Input Diff AND/NAND	INBUF06				OBUF01
EP08	Diff 2–Input XOR/XNOR	INBUF05				OBUF01
EP11	1:2 Diff Fanout buffer	INBUF01				OBUF01
EP16	Diff Receiver	INBUF01				OBUF01
EP31	D Flip Flop with S & R	INBUF02	INBUF03	INBUF08		OBUF01
EP32	2 Divider		INBUF07	INBUF08		OBUF01
EP33	4 Divider		INBUF09	INBUF08		OBUF02
EP35	JK Flip Flop	INBUF10	INBUF11	INBUF12		OBUF01
EP58	2:1 Multiplexer	INBUF03			INBUF02	OBUF01
EP210	Dual 1:5 Clk Distribution	INBUF13				OBUF03

Conventional schematics and net list nomenclature is given in Table 1.

Netlists

```
*List of Input Buffers for EP Family


* Input Buffer
.SUBCKT INBUF01 VCC VEE VCS IN INB Q QB
Q1      2       IN      4       TNA
Q2      2       IN      4       TNA
Q3      3       INB     4       TNA
Q4      3       INB     4       TNA
Q5      4       VCS     5       TNA
Q6      4       VCS     5       TNA
Q7      VCC     2       QB      TNA
Q8      VCC     2       QB      TNA
Q9      VCC     2       QB      TNA
Q10     VCC     2       QB      TNA
Q11     QB      VCS     6       TNA
Q12     QB      VCS     6       TNA
Q13     QB      VCS     6       TNA
Q14     QB      VCS     6       TNA
Q15     VCC     3       Q       TNA
Q16     VCC     3       Q       TNA
Q17     VCC     3       Q       TNA
Q18     VCC     3       Q       TNA
Q19     Q       VCS     7       TNA
Q20     Q       VCS     7       TNA
Q21     Q       VCS     7       TNA
Q22     Q       VCS     7       TNA
**********************************
```

```
R1      VCC     1       125     TC=0.26M, 0.9U
R2      1       2       125     TC=0.26M, 0.9U
R3      1       3       125     TC=0.26M, 0.9U
R4      5       VEE     125     TC=0.26M, 0.9U
R5      6       VEE     67      TC=0.26M, 0.9U
R6      7       VEE     67      TC=0.26M, 0.9U


.ENDS INBUF01


* Input Buffer
.SUBCKT INBUF02 VCC VEE VCS IN INB Q QB
Q1      2       IN      4       TNA
Q2      3       INB     4       TNA
Q3      4       VCS     5       TNA
Q4      VCC     2       QB      TNA
Q5      QB      VCS     6       TNA
Q6      VCC     3       Q       TNA
Q7      Q       VCS     7       TNA
*********************************
R1      VCC     1       250     TC=0.26M, 0.9U
R2      1       2       250     TC=0.26M, 0.9U
R3      1       3       250     TC=0.26M, 0.9U
R4      5       VEE     250     TC=0.26M, 0.9U
R5      6       VEE     250     TC=0.26M, 0.9U
R6      7       VEE     250     TC=0.26M, 0.9U


.ENDS INBUF02


* Input Buffer
.SUBCKT INBUF03 VCC VEE VCS IN INB Q QB
Q1      2       IN      4       TNA
Q2      3       INB     4       TNA
Q3      4       VCS     5       TNA
*********************************
R1      VCC     1       250     TC=0.26M, 0.9U
R2      1       2       250     TC=0.26M, 0.9U
R3      1       3       250     TC=0.26M, 0.9U
R4      5       VEE     250     TC=0.26M, 0.9U


.ENDS INBUF03


* Input Buffer
.SUBCKT INBUF04 VCC VEE VCS VBB IN0 IN1 IN2 IN3 Q QB
Q1      2       IN0     4       TNA
Q2      2       IN0     4       TNA
Q3      2       IN1     4       TNA
Q4      2       IN1     4       TNA
Q5      2       IN2     4       TNA
Q6      2       IN2     4       TNA
Q7      2       IN3     4       TNA
Q8      2       IN3     4       TNA
Q9      3       VBB     4       TNA
Q10     3       VBB     4       TNA
Q11     5       VCS     6       TNA
Q11A    5       VCS     6       TNA
Q12     VCC     2       QB      TNA
Q13     VCC     2       QB      TNA
Q14     VCC     2       QB      TNA
```

```
Q15     VCC     2       QB      TNA
Q16     VCC     3       Q       TNA
Q17     VCC     3       Q       TNA
Q18     VCC     3       Q       TNA
Q19     VCC     3       Q       TNA
Q20     Q       VCS     7       TNA
Q21     Q       VCS     7       TNA
Q22     Q       VCS     7       TNA
Q23     Q       VCS     7       TNA
Q24     QB      VCS     8       TNA
Q25     QB      VCS     8       TNA
Q26     QB      VCS     8       TNA
Q27     QB      VCS     8       TNA

**********************************
R1       VCC     1       125     TC=0.26M, 0.9U
R2       1       2       167     TC=0.26M, 0.9U
R3       1       3       125     TC=0.26M, 0.9U
R4       6       VEE     125     TC=0.26M, 0.9U
R5       7       VEE     67      TC=0.26M, 0.9U
R6       8       VEE     67      TC=0.26M, 0.9U

.ENDS INBUF04

* Input Buffer
.SUBCKT INBUF05 VCC VEE VCS IN0 IN0B IN1 IN1B Q QB
Q1      2       IN0     3       TNA
Q2      2       IN0     3       TNA
Q3      1       IN0B    3       TNA
Q4      1       IN0B    3       TNA
Q5      1       IN1B    4       TNA
Q6      1       IN1B    4       TNA
Q7      2       IN1     4       TNA
Q8      2       IN1     4       TNA
Q9      VCC     2       QB      TNA
Q10     VCC     2       QB      TNA
Q11     VCC     2       QB      TNA
Q12     VCC     2       QB      TNA
Q13     VCC     1       QB      TNA
Q14     VCC     1       QB      TNA
Q15     VCC     1       QB      TNA
Q16     VCC     1       QB      TNA
Q17     9       IN1     10      TNA
Q18     9       IN1     10      TNA
Q19     8       IN1B    10      TNA
Q20     8       IN1B    10      TNA
Q21     8       IN0     11      TNA
Q22     8       IN0     11      TNA
Q23     9       IN0B    11      TNA
Q24     9       IN0B    11      TNA
Q25     VCC     9       Q       TNA
Q26     VCC     9       Q       TNA
Q27     VCC     9       Q       TNA
Q28     VCC     9       Q       TNA
Q29     VCC     8       Q       TNA
Q30     VCC     8       Q       TNA
Q31     VCC     8       Q       TNA
Q32     VCC     8       Q       TNA
Q33     3       VCS     5       TNA
Q34     3       VCS     5       TNA
```

```
Q35     4       VCS     6       TNA
Q36     4       VCS     6       TNA
Q37     QB      VCS     7       TNA
Q38     QB      VCS     7       TNA
Q39     QB      VCS     7       TNA
Q40     QB      VCS     7       TNA
Q41     10      VCS     12      TNA
Q42     10      VCS     12      TNA
Q43     11      VCS     13      TNA
Q44     11      VCS     13      TNA
Q45     Q       VCS     14      TNA
Q46     Q       VCS     14      TNA
Q47     Q       VCS     14      TNA
Q48     Q       VCS     14      TNA

**********************************
R1       VCC     1       250     TC=0.26M, 0.9U
R2       VCC     1       250     TC=0.26M, 0.9U
R3       VCC     2       250     TC=0.26M, 0.9U
R4       VCC     2       250     TC=0.26M, 0.9U
R5       5       VEE     250     TC=0.26M, 0.9U
R6       5       VEE     250     TC=0.26M, 0.9U
R7       5       15      250     TC=0.26M, 0.9U
R8       15      VEE     250     TC=0.26M, 0.9U
R9       6       VEE     250     TC=0.26M, 0.9U
R10      6       VEE     250     TC=0.26M, 0.9U
R11      6       16      250     TC=0.26M, 0.9U
R12      16      VEE     250     TC=0.26M, 0.9U
R13      7       VEE     250     TC=0.26M, 0.9U
R14      7       VEE     250     TC=0.26M, 0.9U
R15      7       VEE     250     TC=0.26M, 0.9U
R16      7       VEE     250     TC=0.26M, 0.9U
R17      VCC     8       250     TC=0.26M, 0.9U
R18      VCC     8       250     TC=0.26M, 0.9U
R19      VCC     9       250     TC=0.26M, 0.9U
R20      VCC     9       250     TC=0.26M, 0.9U
R21      12      VEE     250     TC=0.26M, 0.9U
R22      12      VEE     250     TC=0.26M, 0.9U
R23      12      17      250     TC=0.26M, 0.9U
R24      17      VEE     250     TC=0.26M, 0.9U
R25      13      VEE     250     TC=0.26M, 0.9U
R26      13      VEE     250     TC=0.26M, 0.9U
R27      13      18      250     TC=0.26M, 0.9U
R28      18      VEE     250     TC=0.26M, 0.9U
R29      14      VEE     250     TC=0.26M, 0.9U
R30      14      VEE     250     TC=0.26M, 0.9U
R31      14      VEE     250     TC=0.26M, 0.9U
R32      14      VEE     250     TC=0.26M, 0.9U

.ENDS INBUF05

* Input Buffer
.SUBCKT INBUF06 VCC VEE VCS IN0 IN0B IN1 IN1B Q QB
Q1      1       IN0     4       TNA
Q2      1       IN0     4       TNA
Q3      2       IN0B    4       TNA
Q4      2       IN0B    4       TNA
Q5      4       VCS     6       TNA
Q6      4       VCS     6       TNA
Q7      3       IN1     5       TNA
```

```
Q8      3       IN1     5       TNA
Q9      2       IN1B    5       TNA
Q10     2       IN1B    5       TNA
Q11     5       VCS     7       TNA
Q12     5       VCS     7       TNA
Q13     VCC     1       QB      TNA
Q14     VCC     1       QB      TNA
Q15     VCC     1       QB      TNA
Q16     VCC     1       QB      TNA
Q17     VCC     3       QB      TNA
Q18     VCC     3       QB      TNA
Q19     VCC     3       QB      TNA
Q20     VCC     3       QB      TNA
Q21     VCC     2       Q       TNA
Q22     VCC     2       Q       TNA
Q23     VCC     2       Q       TNA
Q24     VCC     2       Q       TNA
Q25     QB      VCS     9       TNA
Q26     QB      VCS     9       TNA
Q27     QB      VCS     9       TNA
Q28     QB      VCS     9       TNA
Q29     Q       VCS     11      TNA
Q30     Q       VCS     11      TNA
Q31     Q       VCS     11      TNA
Q32     Q       VCS     11      TNA

**********************************
R1       VCC     1       250     TC=0.26M, 0.9U
R2       VCC     1       250     TC=0.26M, 0.9U
R3       VCC     3       250     TC=0.26M, 0.9U
R4       VCC     3       250     TC=0.26M, 0.9U
R5       VCC     2       250     TC=0.26M, 0.9U
R6       VCC     2       250     TC=0.26M, 0.9U
R7       6       VEE     250     TC=0.26M, 0.9U
R8       6       VEE     250     TC=0.26M, 0.9U
R9       7       VEE     250     TC=0.26M, 0.9U
R10      7       VEE     250     TC=0.26M, 0.9U
R11      9       VEE     250     TC=0.26M, 0.9U
R12      9       VEE     250     TC=0.26M, 0.9U
R13      9       VEE     250     TC=0.26M, 0.9U
R14      9       VEE     250     TC=0.26M, 0.9U
R15      11      VEE     250     TC=0.26M, 0.9U
R16      11      VEE     250     TC=0.26M, 0.9U
R17      11      VEE     250     TC=0.26M, 0.9U
R18      11      VEE     250     TC=0.26M, 0.9U

.ENDS INBUF06

* Input Buffer
.SUBCKT INBUF07 VCC VEE VCS IN INB Q QB
Q1      3       IN      5       TNA
Q2      4       INB     5       TNA
Q3      VCC     3       QB      TNA
Q4      VCC     4       Q       TNA
Q5      5       VCS     6       TNA
Q6      QB      VCS     7       TNA
Q7      Q       VCS     8       TNA

**********************************
```

```
R1      VCC     1       250     TC=0.26M, 0.9U
R2      1       2       250     TC=0.26M, 0.9U
R3      1       2       250     TC=0.26M, 0.9U
R4      1       2       250     TC=0.26M, 0.9U
R5      2       3       250     TC=0.26M, 0.9U
R6      2       4       250     TC=0.26M, 0.9U
R7      6       VEE     250     TC=0.26M, 0.9U
R8      7       VEE     250     TC=0.26M, 0.9U
R9      8       VEE     250     TC=0.26M, 0.9U

.ENDS INBUF07

.SUBCKT INBUF08 VCC VEE VCS IN Q
Q1      VCC     IN      4       TNA
Q2      3       VBB     4       TNA
Q3      VCC     3       Q       TNA
Q4      4       VCS     5       TNA
Q5      Q       VCS     6       TNA

**********************************
R1      VCC     1       250     TC=0.26M, 0.9U
R2      1       2       250     TC=0.26M, 0.9U
R3      2       3       250     TC=0.26M, 0.9U
R4      5       VEE     250     TC=0.26M, 0.9U
R5      6       VEE     250     TC=0.26M, 0.9U

.ENDS INBUF08

* Input Buffer
.SUBCKT INBUF09 VCC VEE VCS IN INB Q QB
Q1      3       IN      5       TNA
Q2      4       INB     5       TNA
Q3      VCC     3       QB      TNA
Q4      VCC     4       Q       TNA
Q5      5       VCS     6       TNA
Q6      QB      VCS     7       TNA
Q7      Q       VCS     8       TNA

**********************************
R1      VCC     1       250     TC=0.26M, 0.9U
R2      1       2       250     TC=0.26M, 0.9U
R3      1       2       250     TC=0.26M, 0.9U
R4      2       3       250     TC=0.26M, 0.9U
R5      2       4       250     TC=0.26M, 0.9U
R6      6       VEE     250     TC=0.26M, 0.9U
R7      7       VEE     250     TC=0.26M, 0.9U
R8      8       VEE     250     TC=0.26M, 0.9U

.ENDS INBUF09

* Input Buffer
.SUBCKT INBUF10 VCC VEE VCS VBB JIN KIN J JB K KB
Q1      KB      KIN     2       TNA
Q2      KB      KIN     2       TNA
Q3      K       VBB     2       TNA
Q4      K       VBB     2       TNA
Q5      2       VCS     3       TNA
```

```
Q6      2       VCS     3       TNA
Q7      J       VBB     5       TNA
Q8      J       VBB     5       TNA
Q9      JB      JIN     5       TNA
Q10     JB      JIN     5       TNA
Q11     5       VCS     6       TNA
Q12     5       VCS     6       TNA

**********************************
R1      VCC     1       200     TC=0.26M, 0.9U
R2      1       KB      250     TC=0.26M, 0.9U
R3      1       KB      250     TC=0.26M, 0.9U
R4      1       K       250     TC=0.26M, 0.9U
R5      1       K       250     TC=0.26M, 0.9U
R6      3       VEE     250     TC=0.26M, 0.9U
R7      3       VEE     250     TC=0.26M, 0.9U
R8      VCC     4       200     TC=0.26M, 0.9U
R9      4       J       250     TC=0.26M, 0.9U
R10     4       J       250     TC=0.26M, 0.9U
R11     4       JB      250     TC=0.26M, 0.9U
R12     4       JB      250     TC=0.26M, 0.9U
R13     6       VEE     250     TC=0.26M, 0.9U
R14     6       VEE     250     TC=0.26M, 0.9U

.ENDS INBUF10

* Input Buffer
.SUBCKT INBUF11 VCC VEE VCS VBB IN Q QB
Q1      4       IN      6       TNA
Q2      4       IN      6       TNA
Q3      5       VBB     6       TNA
Q4      5       VBB     6       TNA
Q5      6       VCS     7       TNA
Q6      6       VCS     7       TNA
Q7      VCC     5       Q       TNA
Q8      VCC     5       Q       TNA
Q9      VCC     4       QB      TNA
Q10     VCC     4       QB      TNA
Q11     Q       VCS     9       TNA
Q12     Q       VCS     9       TNA
Q13     QB      VCS     10      TNA
Q14     QB      VCS     10      TNA

**********************************
R1      VCC     11      250     TC=0.26M, 0.9U
R2      VCC     11      250     TC=0.26M, 0.9U
R3      VCC     11      250     TC=0.26M, 0.9U
R4      VCC     11      250     TC=0.26M, 0.9U
R5      11      1       250     TC=0.26M, 0.9U
R6      1       2       250     TC=0.26M, 0.9U
R7      1       2       250     TC=0.26M, 0.9U
R8      2       4       250     TC=0.26M, 0.9U
R9      1       4       250     TC=0.26M, 0.9U
R10     1       5       250     TC=0.26M, 0.9U
R11     1       3       250     TC=0.26M, 0.9U
R12     1       3       250     TC=0.26M, 0.9U
R13     3       5       250     TC=0.26M, 0.9U
R14     7       8       250     TC=0.26M, 0.9U
R15     8       VEE     250     TC=0.26M, 0.9U
```

```
R16     7       VEE     250     TC=0.26M, 0.9U
R17     9       VEE     250     TC=0.26M, 0.9U
R18     9       VEE     250     TC=0.26M, 0.9U
R19     10      VEE     250     TC=0.26M, 0.9U
R20     10      VEE     250     TC=0.26M, 0.9U


.ENDS INBUF11


* Input Buffer
.SUBCKT INBUF12 VCC VEE VCS IN Q
Q1      9       IN      11      TNA
Q2      10      VBB     11      TNA
Q3      11      VCS     12      TNA
Q4      VCC     10      Q       TNA
Q5      VCC     10      Q       TNA
Q6      Q       VCS     13      TNA
Q7      Q       VCS     13      TNA

**********
R1      VCC     2       250     TC=0.26M, 0.9U
R2      VCC     1       250     TC=0.26M, 0.9U
R3      1       2       250     TC=0.26M, 0.9U
R4      VCC     2       250     TC=0.26M, 0.9U
R5      2       3       250     TC=0.26M, 0.9U
R6      2       3       250     TC=0.26M, 0.9U
R7      2       4       250     TC=0.26M, 0.9U
R8      2       4       250     TC=0.26M, 0.9U
R9      3       5       250     TC=0.26M, 0.9U
R10     4       6       250     TC=0.26M, 0.9U
R11     5       7       250     TC=0.26M, 0.9U
R12     6       8       250     TC=0.26M, 0.9U
R13     7       9       250     TC=0.26M, 0.9U
R14     8       10      250     TC=0.26M, 0.9U
R15     12      VEE     250     TC=0.26M, 0.9U
R16     13      VEE     250     TC=0.26M, 0.9U
R17     13      VEE     250     TC=0.26M, 0.9U


.ENDS INBUF12


* Input Buffer
.SUBCKT INBUF13 VCC VEE VCS IN INB Q QB
Q1      QB      IN      1       TNA
Q2      QB      IN      1       TNA
Q3      QB      IN      1       TNA
Q4      QB      IN      1       TNA
Q5      Q       INB     1       TNA
Q6      Q       INB     1       TNA
Q7      Q       INB     1       TNA
Q8      Q       INB     1       TNA
Q9      1       VCS     2       TNA
Q10     1       VCS     2       TNA
Q11     1       VCS     2       TNA
Q12     1       VCS     2       TNA

**********
R1      VCC     QB      214     TC=0.26M, 0.9U
R2      VCC     Q       214     TC=0.26M, 0.9U
R3      2       VEE     125     TC=0.26M, 0.9U
```

```
.ENDS INBUF13


* Output Buffer
.SUBCKT OBUF01 VCC VEE VCS IN INB Q QB
Q1      1       IN      3       TNB
Q2      1       IN      3       TND
Q3      1       IN      3       TND
Q4      2       INB     3       TND
Q5      2       INB     3       TND
Q6      2       INB     3       TNB
Q7      3       VCS     4       TND
Q8      3       VCS     4       TND
Q9      3       VCS     4       TNB
Q10     VCC     1       QB      TNC
Q11     VCC     2       Q       TNC
************************************
R1      VCC     1       240     TC=0.26M, 0.9U
R2      VCC     1       240     TC=0.26M, 0.9U
R3      VCC     2       240     TC=0.26M, 0.9U
R4      VCC     2       240     TC=0.26M, 0.9U
R5      4       VEE     225     TC=0.26M, 0.9U
R6      4       VEE     225     TC=0.26M, 0.9U
R7      4       VEE     225     TC=0.26M, 0.9U
R8      4       VEE     225     TC=0.26M, 0.9U
R9      4       VEE     225     TC=0.26M, 0.9U
R10     4       VEE     225     TC=0.26M, 0.9U
R11     4       VEE     225     TC=0.26M, 0.9U
R12     4       VEE     225     TC=0.26M, 0.9U


.ENDS OBUF01


* Output Buffer
.SUBCKT OBUF02 VCC VEE VCS IN INB Q QB
Q1      1       IN      3       TNB
Q2      2       INB     3       TNB
Q3      VCC     1       QB      TNC
Q4      VCC     2       Q       TNC
Q5      3       VCS     4       TNB


************************************
R1      VCC     1       240     TC=0.26M, 0.9U
R2      VCC     2       240     TC=0.26M, 0.9U
R3      4       VEE     225     TC=0.26M, 0.9U
R4      4       VEE     225     TC=0.26M, 0.9U
R5      4       VEE     225     TC=0.26M, 0.9U
R6      4       VEE     225     TC=0.26M, 0.9U


.ENDS OBUF02


* Output Buffer
.SUBCKT OBUF03 VCC VEE VCS IN INB Q QB
Q1      QB      IN      1       TNB
Q2      Q       INB     1       TNB
Q3      1       VCS     2       TNB


************************************
R1      VCC     QB      265     TC=0.26M, 0.9U
```

```
R2      VCC     Q       265     TC=0.26M, 0.9U
R3      2       VEE      18     TC=0.26M, 0.9U


.ENDS OBUF03


* Input ESD
.SUBCKT IN_ESD_PD VCC VEE IN Q
D1      IN      VCC     ESDM
D2      IN      VCC     ESDM
D3      IN      VCC     ESDM
D4      VEE     IN      ESDM
D5      VEE     IN      ESDS
D6      VEE     IN      ESDM
D7      VEE     IN      ESDS
D8      VEE     IN      ESDM
D9      VEE     IN      ESDS
************************************
R1      IN      VEE     75K     TC=1.02M, 1.7U
RB1     IN      Q       185     TC=0.26M, 0.9U
RB2     IN      Q       185     TC=0.26M, 0.9U


.ENDS IN_ESD_PD


* Output ESD
.SUBCKT OUT_ESD VCC VEE Q
D1      Q       VCC     ESDM
D2      Q       VCC     ESDM
D3      VEE     Q       ESDM
D4      VEE     Q       ESDS
D5      VEE     Q       ESDM
D6      VEE     Q       ESDS


.ENDS OUT_ESD


*TEST CIRCUIT


VCC     VCC     0       0V
VEE     VEE     0       –3.3V
VCS     VCS     0       –2.2V
VTT     VTT     0       –2.0V
VBB     VBB     0       –1.250V
RBB     VBB     0       1MEG
VIN     IN      0       PULSE(–1.7 –0.95 5NS 5NS 5NS 50NS 110NS)
VINB    INB     0       PULSE(–0.95 –1.7 5NS 5NS 5NS 50NS 110NS)


.GROUND 0
.TRAN   0.2NS   120NS
XIN     VCC     VEE     VCS     1       2       3       4       INBUF01
XOUT    VCC     VEE     VCS     3       4       Q       QB      OBUF01
XINESD  VCC     VEE     IN      1       IN_ESD_PD
XINESDB VCC     VEE     INB     2       IN_ESD_PD
XOESD   VCC     VEE     Q       OUT_ESD
XOESDB  VCC     VEE     QB      OUT_ESD


RL      Q       VTT     50
RLB     QB      VTT     50
```

```
********* MOSAIC V TRANSISTOR NOMINAL SPICE MODELS REV4.6 5/18/99 **********


*******************************************************************************
.MODEL TNA NPN (IS=6.54e-18 BF=195 NF=1 VAF=93.6 IKF=6.81e-03
+ ISE=3.26e-16 NE=2.5 BR=18.4 VAR=2.76 IKR=6.36e-04 ISC=1.89e-17
+ NC=1.426 RB=544 IRB=3.16e-05 RBM=154 RE=13 RC=61 CJE=1.45e-14
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=5.2e-03 XTF=2.8 VTF=1.4 PTF=41.56 TR=1e-9
+ CJC=5.68e-15 VJC=0.632 MJC=0.301 XCJC=.3 CJS=7.94e-15 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*******************************************************************************
*******************************************************************************
.MODEL TND NPN (IS=1.09e-17 BF=185 NF=1 VAF=95.5 IKF=1.18e-02
+ ISE=3.43e-16 NE=2.5 BR=19.5 VAR=2.76 IKR=1.02e-03 ISC=2.18e-17
+ NC=1.426 RB=389 IRB=5.45e-05 RBM=94 RE=10 RC=41 CJE=2.46e-14
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=8.5e-03 XTF=2.8 VTF=1.4 PTF=41.56 TR=1e-9
+ CJC=8.49e-15 VJC=0.632 MJC=0.301 XCJC=.3 CJS=1.06e-14 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*******************************************************************************
*******************************************************************************
.MODEL TNC NPN (IS=1.47e-16 BF=180 NF=1 VAF=96.3 IKF=1.62e-01
+ ISE=2.96e-15 NE=2.5 BR=20.2 VAR=2.76 IKR=1.34e-02 ISC=2.14e-16
+ NC=1.426 RB=96 IRB=1.50e-03 RBM=4 RE=1 RC=14 CJE=3.34e-13
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=1.1e-01 XTF=2.8 VTF=1.4 PTF=41.56 TR=1e-9
+ CJC=1.08e-13 VJC=0.632 MJC=0.301 XCJC=.3 CJS=8.12e-14 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*******************************************************************************
*******************************************************************************
.MODEL TNB NPN (IS=2.18e-17 BF=179 NF=1 VAF=96.5 IKF=2.42e-02
+ ISE=3.83e-16 NE=2.5 BR=20.4 VAR=2.76 IKR=1.98e-03 ISC=2.91e-17
+ NC=1.426 RB=230 IRB=1.12e-04 RBM=48 RE=6 RC=22 CJE=4.98e-14
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=1.6e-02 XTF=2.8 VTF=1.4 PTF=41.56 TR=1e-9
+ CJC=1.55e-14 VJC=0.632 MJC=0.301 XCJC=.3 CJS=1.71e-14 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*******************************************************************************
*******************************************************************************
.MODEL ESDM D (IS=1.55E-14 CJO=160fF RS=12 VJ=.58 M=.25 BV=9)
*******************************************************************************
.MODEL ESDS D (IS=1.55E-14 CJO=29fF VJ=.624 M=.571)
*******************************************************************************


.END
```

EPT SPICE Modeling Kit

Prepared by
Paul Shockman
ON Semiconductor Logic Applications Engineering

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

APPLICATION NOTE

Objective

The objective of this kit is to provide customers with enough schematic and SPICE parameter information to perform system level interconnect modeling with the ON Semiconductor ECLinPS Plus™ Translator EPT family. The EPT devices MC100EPT2xD are single or dual supply 1 or 2 Bit translators between the TTL and ECL/PECL worlds. Single supply devices translate between TTL and PECL, dual supply devices translate to or from negative supplied ECL. All devices are designed as 100K compatible 100EPT2x.

The kit contains representative schematics and model files for the I/O circuits used by the EPT20 and EPT22 devices. The package model should be placed on all external inputs, outputs and supply pins.

Input and Output Schematics

The TTL–PECL Translator function uses circuit schematics LVTTL01 and LVTTL02 for references diagrams to the SPICE netlists.

All inputs and outputs of the ELT family are protected by ESD protection circuitry. The ESD circuit, IN_ESD, is used for TTL Input and OUT_ESD for PECL outputs.

If the user would like to just simulate the output behavior of an TTL output the TTL_OUT circuit can be stimulated with internal signals.

To all external pins the package model, LINES, needs to be added. If users want to reduce simulation time and just simulate 1 channel or only the output of a circuit, they need to take care of the correct power supply management. The channels share power supply pins. Dynamic ICC current will add up at power pins. When a simulation is performed with only one channel, the package models of the power pins need to be adjusted. The parasitic capacitance and inductance should be adjusted accordingly.

Modeling

The bias driver schematics for VCS and V1 generation are not included in this kit, as they are unnecessary for interconnection simulation. In addition their use would result in a relatively large in simulation time. Alternatively the internal reference voltages should be driven with ideal constant voltage sources.

Parameter	Typical Level	Worst Case
VCS	VEE+1.3V	±50mV
V1	VEE+2.1V	±50mV

This model kit is intended for simulations within the specified power supply range. If supply voltages drop below minimum specification, VCS and V1 can no longer be assumed to be constant. Thus, this model kit can not be used for power up or power down simulations. The 10K ohm resistor should NOT be simulated as simple SPICE resistor because it is fabricated by a diffusion step in wafer processing and there is an associated parasitic. The following subcircuit should be used to enhance the performance of the simulation.

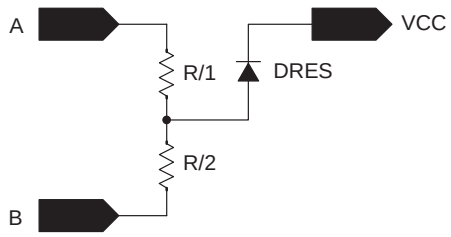


Figure 1. Resistor Model

```
.SUBCKT RESK A B VCC params: R=10000
* Assumes Sheet Rho=500OHM, Resistor Width=10U, and Cap in Farads.
Ra A 1 {R/2} TC=900U
Rb 1 B {R/2} TC=900U
D1 1 VCC DRES
.MODEL DRES D
+ (IS=3.7E–16
+ CJO=0.265E–16*R+29E–16)
.ENDS RESK
```

The nodes in the model files and the schematics are:

Name	Node	Description
VCC	100	3.3V High rail power supply
VEE	200	0.0V Lowest Rail Power supply
VCS	300	1.24 Current Source Base Voltage (VEE+1.3V)V
V1	400	2.1 Internal TTL Transfer Reference Supply
VTT	500	1.3V External termination sink supply (VCC—2V)
VIN	51	PULSE (.8 to 2.0, tr/tf 5NS, PW 20NS, PER 50NS)

Temperature coefficients are annotated (* TC=).

For typical load ECL and PECL outputs should be terminated 50ohm to VTT=VCC—2V. TTL outputs are loaded with 20pF to GROUND and 500OHM to GROUND.

***

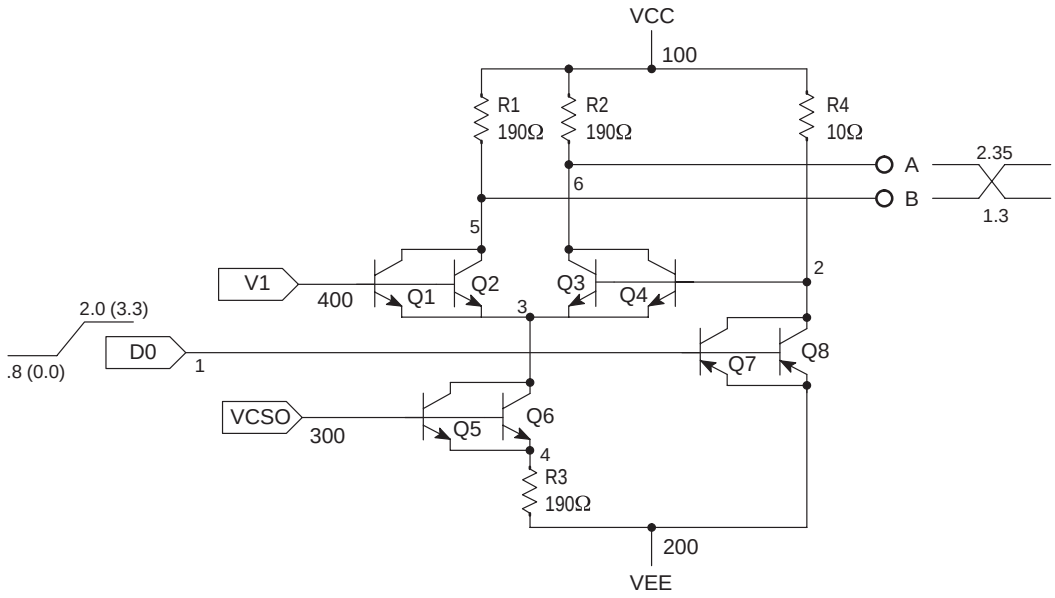


Figure 2. LVTTL–LVPECL Translator
EPT20/22
LVPECL output

For LVTTL01, the following transitors are used:

```
Q1   TRANA
Q2   TRANA
Q3   TRANA
Q4   TRANA
Q5   TRANA
Q6   TRANA
Q7   TRANE
Q8   TRANE
```

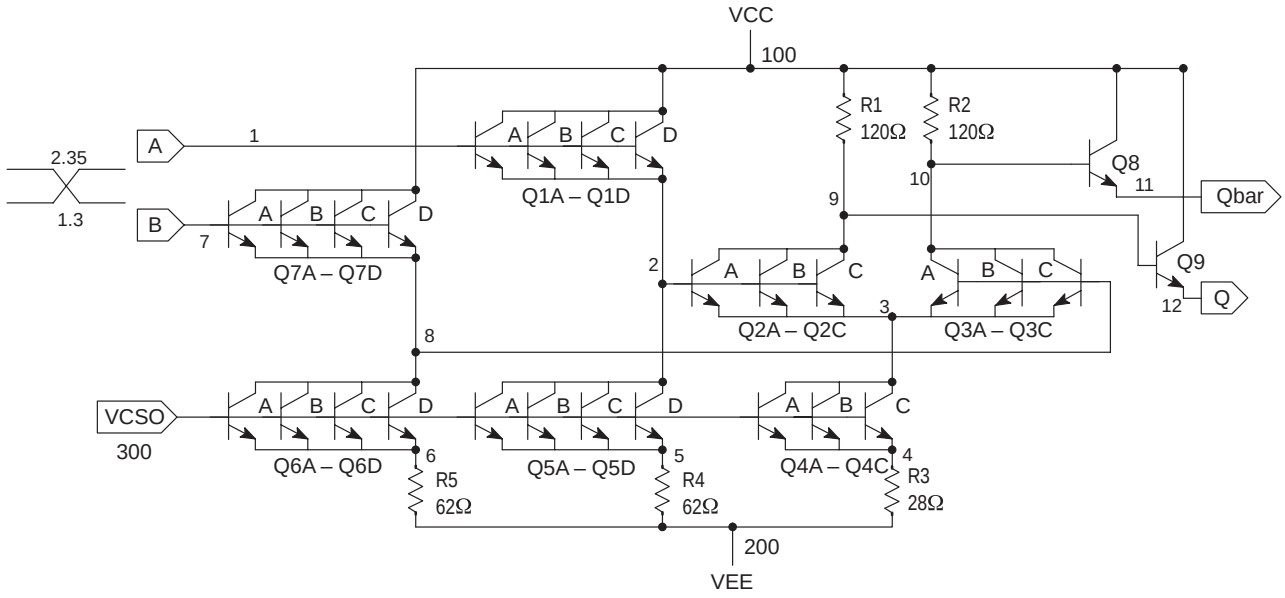


Figure 3. LVTTL–LVPECL Translator
EPT20/22
LVPECL output

For LVTTL02 the following transitors are used:

```
Q1A–D  TRANA
Q2A–C  TRANB
Q3A–C  TRANB
Q4A–C  TRANB
Q5A–D  TRANA
Q6A–D  TRANA
Q7A–D  TRANA
Q8     TRAND
Q9     TRAND
```

```
.TRAN     0.2NS  120NS
XLVTTL01  100    200   300   400     1       5    6   LVTTL01
XLVTTL02  100    200   300   5       6       11   12  LVTTL02
XINESD    100    200   51    1       IN_ESD
XOUTESD   100    200   11    OUT_ESD
XOUTESDB  100    200   12    OUT_ESD
XQBTERM   500    12    RTERM
XQTERM    500    11    RTERM
```

```
.SUBCKT LVTTL01 100 200 300 400 1 5 6
Q1  5    400 3   200  TRANA
Q2  5    400 3   200  TRANA
Q3  6    2   3   200  TRANA
Q4  6    2   3   200  TRANA
Q5  3    300 4   200  TRANA
Q6  3    300 4   200  TRANA
Q7  2    1   200 200  TLS
Q8  2    1   200 200  TLS
R1  100  5   190
* TC=0.26M, 0.9U
R2  100  6   190
```

```
* TC=0.26M, 0.9U
R3  4    200 190
* TC=0.26M, 0.9U
R4  100  2   10000
* TC=0.26M, 0.9U
.ENDS LVTTL01


.SUBCKT LVTTL02 100 200 300 1 7  11 12
Q1A  100   1  2  200 TRANA
Q1B  100   1  2  200 TRANA
Q1C  100   1  2  200 TRANA
Q1D  100   1  2  200 TRANA
Q2A    9   2   3 200  TRANB
Q2B    9   2   3 200  TRANC
Q2C    9   2   3 200  TRANC
Q3A   10   8   3 200  TRANB
Q3B   10   8   3 200  TRANC
Q3C   10   8   3 200  TRANC
Q4A    3  300  4 200  TRANB
Q4B    3  300  4 200  TRANB
Q4C    3  300  4 200  TRANB
Q5A    2  300  5 200  TRANA
Q5B    2  300  5 200  TRANA
Q5C    2  300  5 200  TRANA
Q5D    2  300  5 200  TRANA
Q6A    8  300  6 200  TRANA
Q6B    8  300  6 200  TRANA
Q6C    8  300  6 200  TRANA
Q6D    8  300  6 200  TRANA
Q7A  100   7   8 200  TRANA
Q7B  100   7   8 200  TRANA
Q7C  100   7   8 200  TRANA
Q7D  100   7   8  200  TRANA
Q8   100  10   11 200  TRAND
Q9   100   9   12 200  TRAND
R1   100   9   120
* TC=0.26M, 0.9U
R2   100  10   120
* TC=0.26M, 0.9U
R3     4  200  28
*  TC=0.26M, 0.9U
R4     5  200  62
*  TC=0.26M, 0.9U
R5     6  200  62
*  TC=0.26M, 0.9U
.ENDS LVTTL02


* INPUT ESD   51 = in, 61 out
.SUBCKT IN_ESD 100 200 51 61
D1      51      100     ES14X19M
D2      51      100     ES14X19M
D3      51      100     ES14X19M
D4      200     51      ES14X19M
D5      200     51      ES14X19S
D6      200     51      ES14X19M
D7      200     51      ES14X19S
D8      200     51      ES14X19M
D9      200     51      ES14X19S
RB1     51  61  1000
*     TC=0.26M, 0.9U
.ENDS IN_ESD
```

```
* OUTPUT ESD
.SUBCKT OUT_ESD  100  200 81
D1      81      100     ES14X19M
D2      81      100     ES14X19M
D3      200     81      ES14X19M
D4      200     81      ES14X19S
D5      200     81      ES14X19M
D6      200     81      ES14X19S
.ENDS OUT_ESD


.SUBCKT RTERM    500   91
R1  91 500 50
.ENDS

.END

.MODEL TRANA NPN (IS=8.12E-18 BF=192 NF=1 VAF=75.6 IKF=1.49E-02
+ ISE=9.14E-17 NE=2 BR=15.8 VAR=2.76 IKR=2.2E-03 ISC=2.62E-16
+ NC=1.578 RB=327 IRB=4.8E-05 RBM=0.001 RE=10 RC=15 CJE=2.0E-14
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=7.6E-03 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=5.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=4.8E-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)


.MODEL TRANC NPN (IS=1.36E-17 BF=180 NF=1 VAF=87.6 IKF=2.19E-02
+ ISE=6.65E-16 NE=2 BR=16.9 VAR=2.76 IKR=1.5E-03 ISC=1.11E-16
+ NC=1.578 RB=136 IRB=3.24E-05 RBM=0.001 RE=6 RC=8 CJE=1.02E-13
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=1.27E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=10.3E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=9.94E-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)


.MODEL TRAND NPN (IS=6.55E-17 BF=103 NF=1 VAF=90 IKF=2.91E-01
+ ISE=8.85E-15 NE=2 BR=15.7 NR=1 VAR=3.82 IKR=2.01E-02 ISC=1.48E-15
+ NC=2 RB=10.5 IRB=4.39E-04 RBM=0.29 RE=0.351 RC=9 CJE=3.5E-13
+ VJE=.8167 MJE=.1973 TF=8.99E-12 ITF=1.3E-01 XTF=5.67 VTF=1.86 PTF=41.43 TR=6.405E-10
+ CJC=1.4E-13 VJC=.6401 MJC=.2674 XCJC=1 CJS=9.3E-14 VJS=.5002 MJS=.1706
+ EG=1.135 XTI=4.177 XTB=0.6322 FC=0.961)


.MODEL TRANB NPN (IS=2.71E-17 BF=172 NF=1 VAF=71.4 IKF=4.38E-02
+ ISE=1.33E-15 NE=2 BR=17.9 VAR=2.76 IKR=3.0E-03 ISC=2.22E-16
+ NC=1.578 RB=67 IRB=6.47E-05 RBM=0.001 RE=3 RC=4 CJE=5.09E-14
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=2.53E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=20.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=1.7E-14 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)


.MODEL TRANEPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05
+ ISE=7.75e-17 NE=1.813 BR=210 VAR=5.68 IKR=6.51e-05 ISC=7.75e-17
+ NC=1.813 RB=349 IRB=1.77e-07 RBM=53 RE=119 RC=158 CJE=7.04e-15
+ VJE=0.6578 MJE=0.149 TF=6.33e-10 ITF=2.2e-08 XTF=2.8 VTF=1.4
+ PTF=41.56 TR=1e-9 CJC=7.04e-15 VJC=0.8034 MJC=0.1773 XCJC=.3
+ CJS=4.79e-15 VJS=.4193 MJS=0.0902
+ EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9)


.MODEL TLS LPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05
+ ISE=7.75e-17 NE=1.813 BR=210.1 NR=1 VAR=5.68 IKR=2.61e-04 ISC=7.75e-17
+ NC=1.813 RB=349 IRB=1.8e-07 RBM=53 RE=119 RC=158 CJE=7.0e-15
+ VJE=.6578 MJE=.149 TF=6.33e-10 ITF=2.2e-08 XTF=.5356 VTF=.2365 PTF=0 TR=6.33e-10
+ CJC=7.0e-15 VJC=.8034 MJC=.1773 XCJC=1 CJS=4.8e-15 VJS=.5 MJS=.09022
+ EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9)
```

```
.MODEL ES14X19M D (IS=1.55E-14 CJO=160FF RS=12 VJ=.58 M=.25 BV=9)


.MODEL ES14X19S D (IS=1.55E-14 CJO=29FF VJ=.624 M=.571)
.END


* PACKAGE: 8SOIC
* SPICE SUBCIRCUIT FILE OF COUPLED TRANSMISSION LINES
* CREATED FRI APR 25 16:47:54 1997
* BY PMG VERSION 3.6.2
*
* TRANSMISSION LINE MODEL
*   CONDUCTOR     PIN
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*
* NUMBER OF LUMPS:      1
* FASTEST APPLICABLE EDGE RATE:         0.076 NS
* CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
*
.SUBCKT LINES N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O
L01WB   N01I    N01M    1.367E-09
L01     N01M    N01O    7.794E-10
C01     N01M    0       2.445E-13
L02WB   N02I    N02M    1.287E-09
L02     N02M    N02O    5.473E-10
C02     N02M    0       1.888E-13
L03WB   N03I    N03M    1.287E-09
L03     N03M    N03O    5.473E-10
C03     N03M    0       1.901E-13
L04WB   N04I    N04M    1.367E-09
L04     N04M    N04O    7.723E-10
C04     N04M    0       2.443E-13
L05WB   N05I    N05M    1.367E-09
L05     N05M    N05O    7.710E-10
C05     N05M    0       2.478E-13
L06WB   N06I    N06M    1.287E-09
L06     N06M    N06O    5.489E-10
C06     N06M    0       1.916E-13
L07WB   N07I    N07M    1.287E-09
L07     N07M    N07O    5.495E-10
C07     N07M    0       1.930E-13
L08WB   N08I    N08M    1.367E-09
L08     N08M    N08O    7.786E-10
C08     N08M    0       2.451E-13
K0102   L01     L02     0.1687
K0102WB L01WB   L02WB   0.3400
C0102   N01O    N02O    3.674E-14
K0103   L01     L03     0.0702
K0103WB L01WB   L03WB   0.1847
K0203   L02     L03     0.1822
K0203WB L02WB   L03WB   0.3505
C0203   N02O    N03O    3.521E-14
K0204   L02     L04     0.0682
K0204WB L02WB   L04WB   0.1847
```

```
K0304   L03     L04     0.1694
K0304WB L03WB   L04WB   0.3400
C0304   N03O    N04O    3.675E−14
K0305WB L03WB   L05WB   0.1847
K0405WB L04WB   L05WB   0.3455
K0406WB L04WB   L06WB   0.1847
K0506   L05     L06     0.1697
K0506WB L05WB   L06WB   0.3400
C0506   N05O    N06O    3.720E−14
K0507   L05     L07     0.0682
K0507WB L05WB   L07WB   0.1847
K0607   L06     L07     0.1824
K0607WB L06WB   L07WB   0.3505
C0607   N06O    N07O    3.570E−14
K0608   L06     L08     0.0702
K0608WB L06WB   L08WB   0.1847
K0708   L07     L08     0.1691
K0708WB L07WB   L08WB   0.3400
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.ENDS LINES
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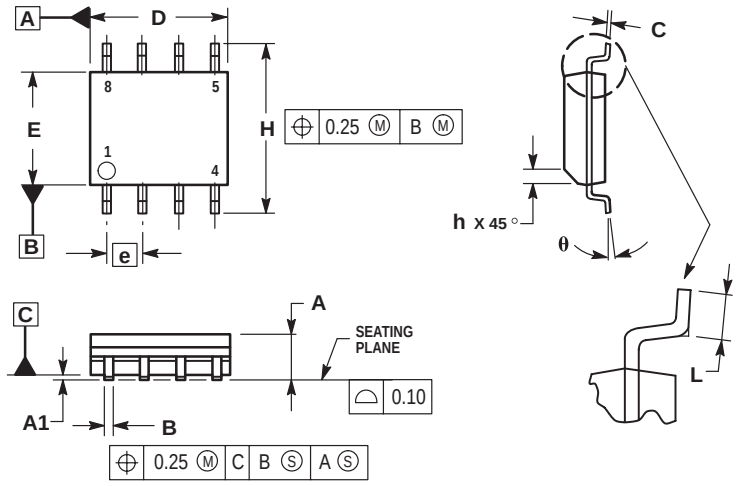
Package Specifications

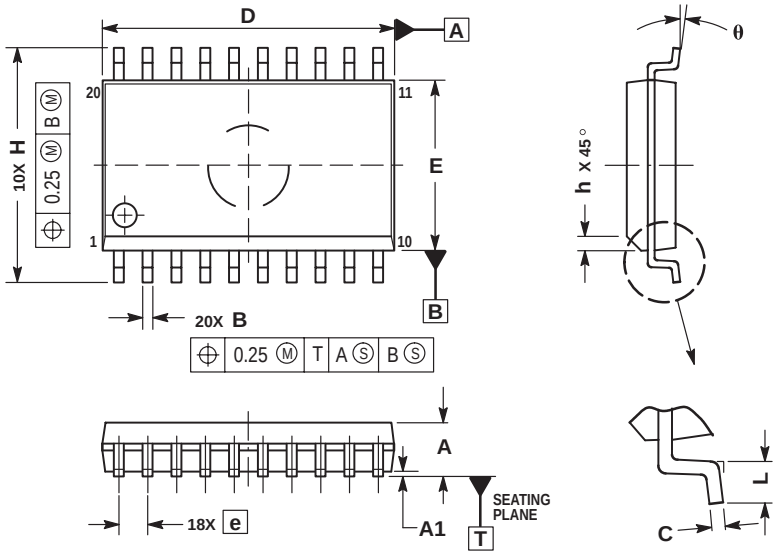
CASE OUTLINE AND PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

SO–8
CASE 751–06
ISSUE T

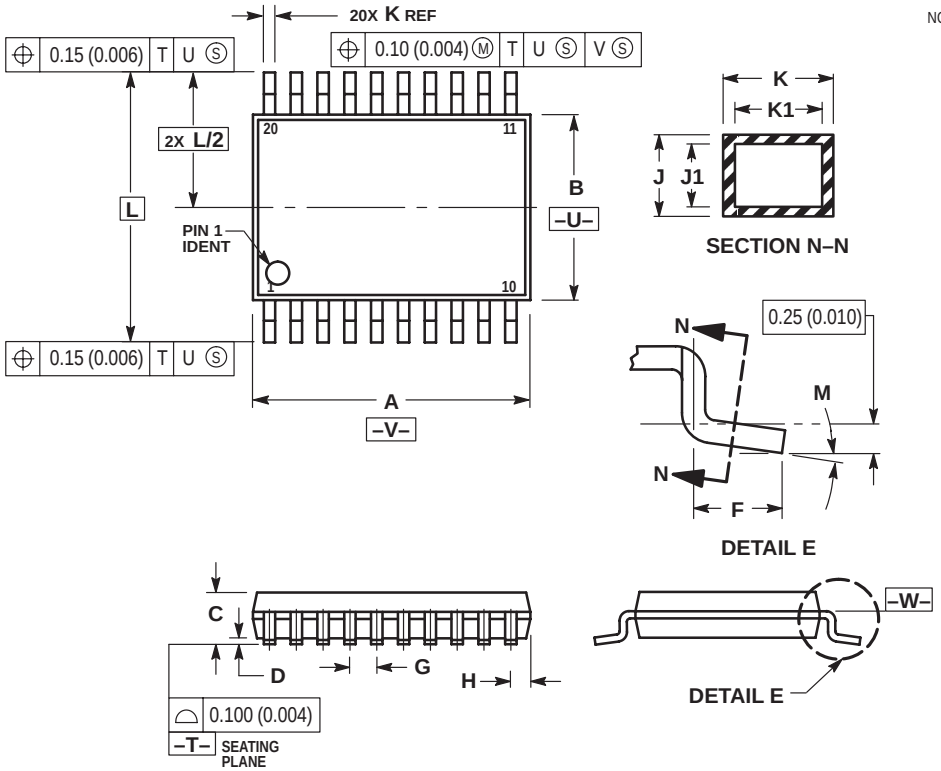


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

SO–20
CASE 751D–05
ISSUE F

CASE OUTLINE AND PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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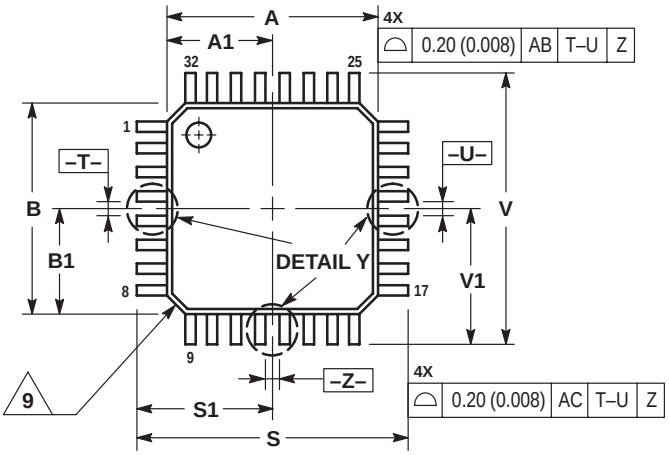
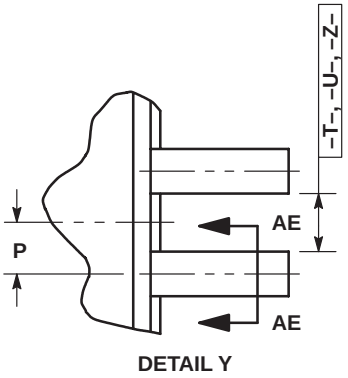
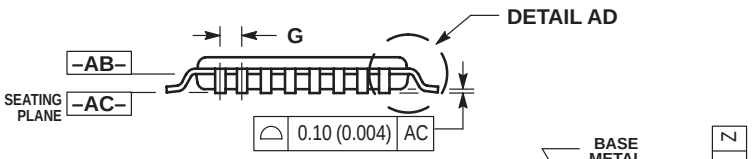
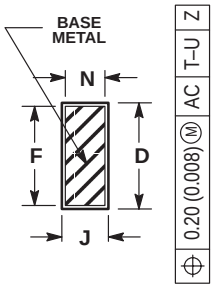
CASE OUTLINE AND PACKAGE DIMENSIONS



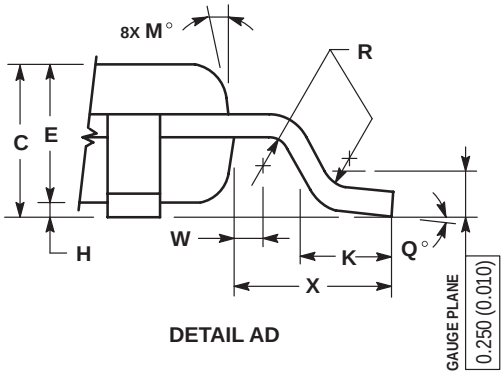


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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* Majority of information (> 60%) is procedural, not functional, in nature
* Volume of information is typically less than for Reference Manuals
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